INTEL XEON SCALABLE (SKYLAKE) PROCESSOR AND PURLEY PLATFORM

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Agenda

SuperMUC-NG system overview

Purley Platform Features

Skylake processor

- Uncore Architecture
- Core Architecture

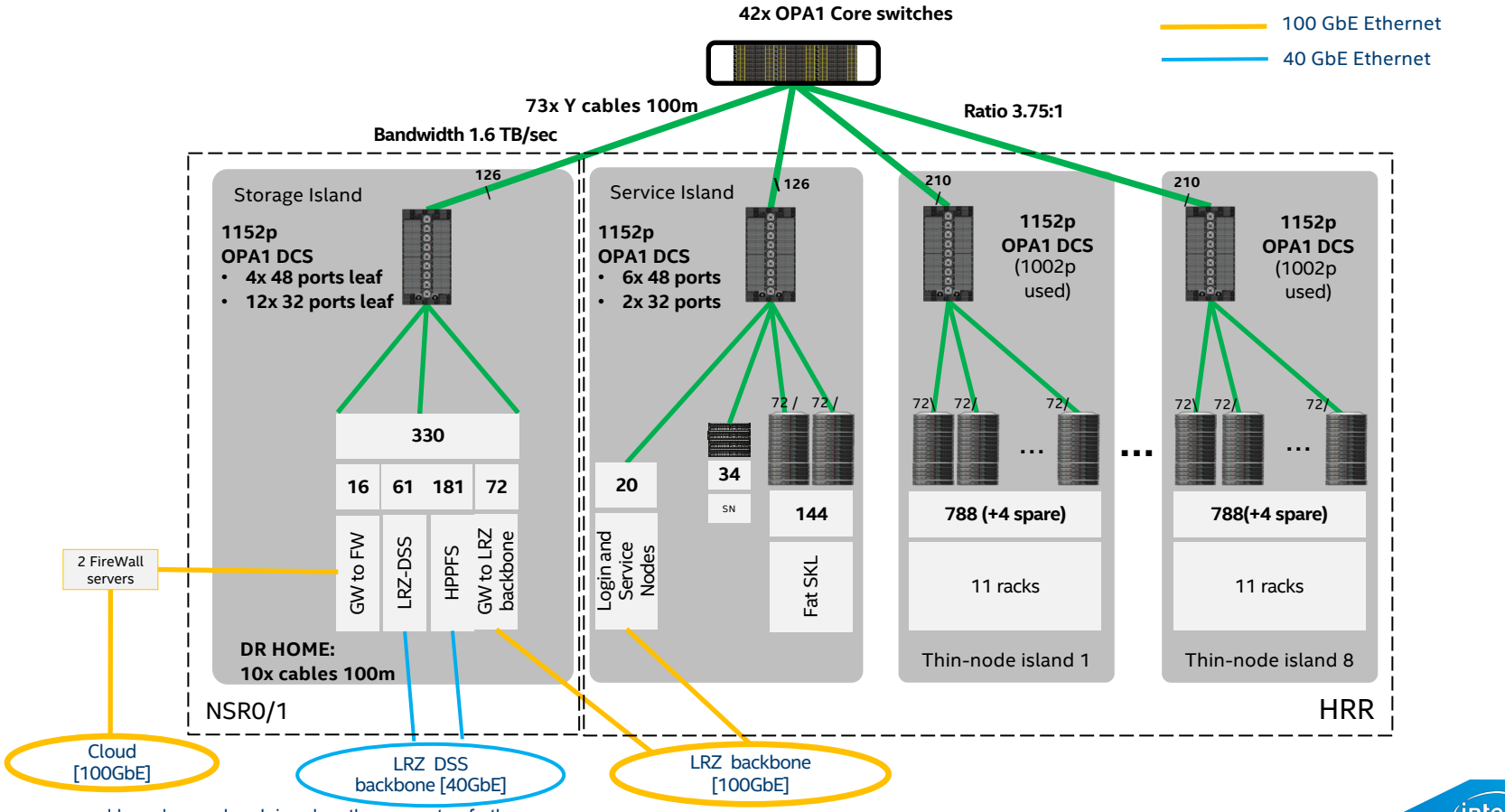
Some abbreviations used in the presentation:
AVX – Advanced Vector Extensions
ISA – Instruction Set Architecture
SKX – Skylake Server, also Skylake-SP: codename for Intel Xeon Scalable Processor
LBG – Lewisburg: codename for Intel C620 Series Chipsets
MLC – Mid-Level Cache, usually 2nd level cache
LLC – Last Level Cache, usually Level-3 cache of a processor
OPA – Intel Omni-Path Architecture fabric
UPI – Intel Ultra Path Interconnect
QPI – Intel QuickPath Interconnect

Characteristics of SuperMUC-NG

Compute Nodes	Thin Nodes	Fat Nodes	Total (Thin + Fat)
Processor	Intel Xeon Platinum 8174 (Skylake-SP)		
Cores per Node	48	48	
Memory per node (GByte)	96	768	
Number of Nodes	6'336	144	6'480
Number of Cores	304'128	8'912	311'040
Rpeak @ nominal (PFlop/s)	26.3	0.6	26.9
Memory (TByte)	608	111	719
High-Performance Fabric			
Intel Omni-Path Architecture fabric	"Inverted" fat tree: 8 thin-node islands non-blocking within 792 nodes		
Filesystems			
High Performance Parallel Filesystem (HPPFS)	50 PB @ 500 GB/s for $SCRATCH and $WORK		
Data Science Storage (DSS)	20 PB @ 70 GB/s for $PROJECT		
Home Filesystem	256 TB for $HOME		
Infrastructure			
Cooling	Direct warm water cooling		
Waste Heat Reuse	Reuse for producing cold water with adsorption coolers		
Software			
Operating system and provisioning	SuSE Linux (SLES 12 SP3) and xCat, OpenHPC-compliant, network boot		
Batch system, containers	SLURM 18.08, containers (e.g., CharlieCloud, etc.)		
Development Environment	Intel Parallel Studio XE 2019, Intel MPI 2019		

Source: https://www.lrz.de/services/compute/supermuc/supermuc-ng/

System design: islands and fabrics



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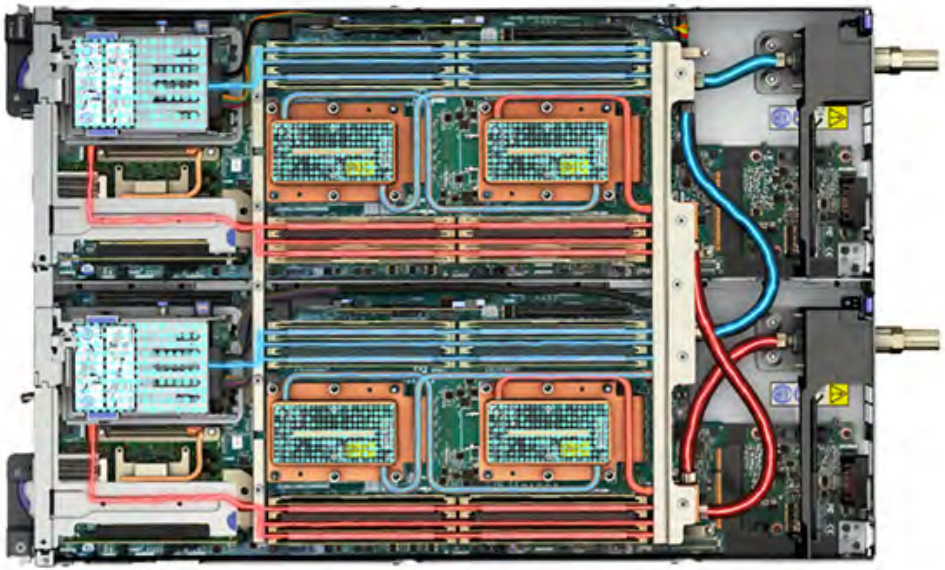
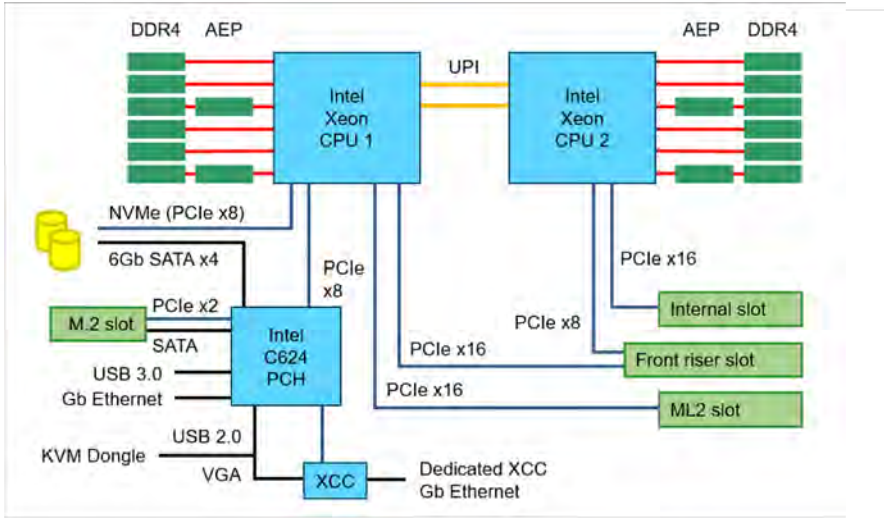
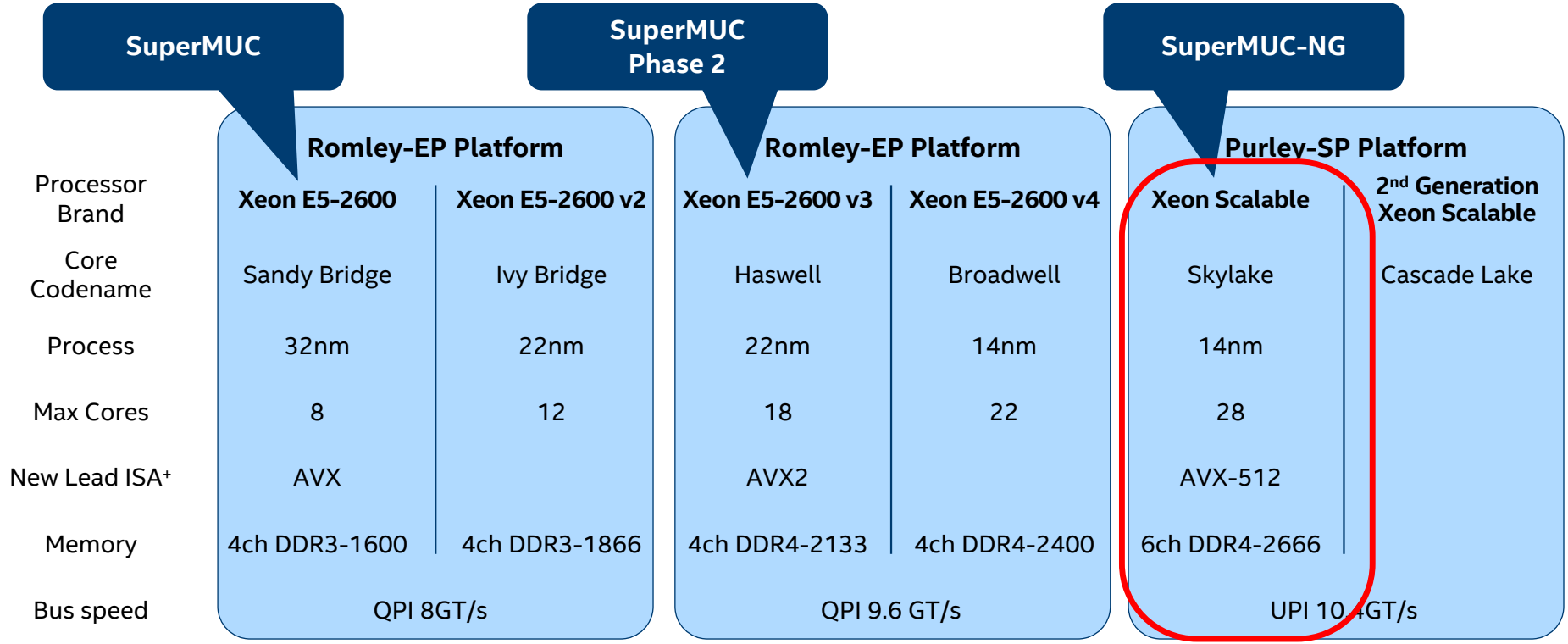
System design: compute node and chassis





Source: Lenovo, and HPCWire https://www.hpcwire.com/2018/02/22/lenovo-unveils-warm-water-cooled-thinksystem-sd650-rampup-lrz-install/

Intel Server Platforms Transitions



Source: https://ark.intel.com

+ All processors support prior available x86 ISA extensions up to Intel® SSE4.2 and several application-specific accelerator instructions, such as AES-NI

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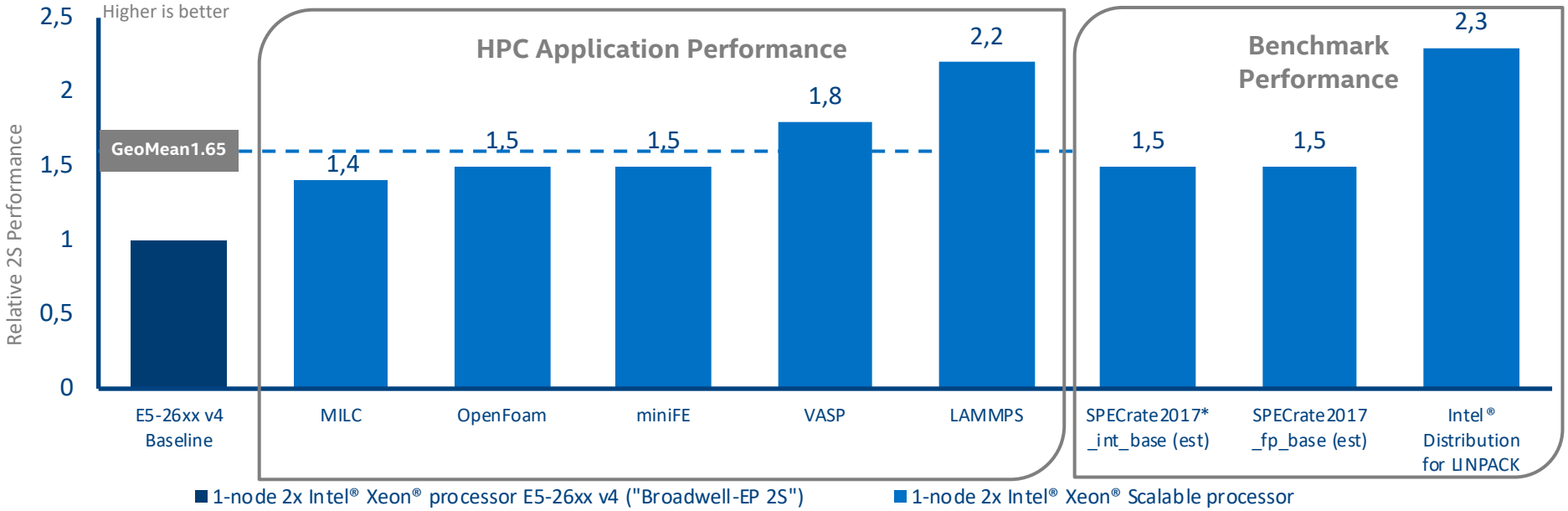
Significant Performance Gains on HPC Applications

Intel® Xeon® Scalable Processor



Performance results are based on testing as of June 2018 and may not reflect all publicly available security updates. See configuration disclosure for details. No product can be absolutely secure.
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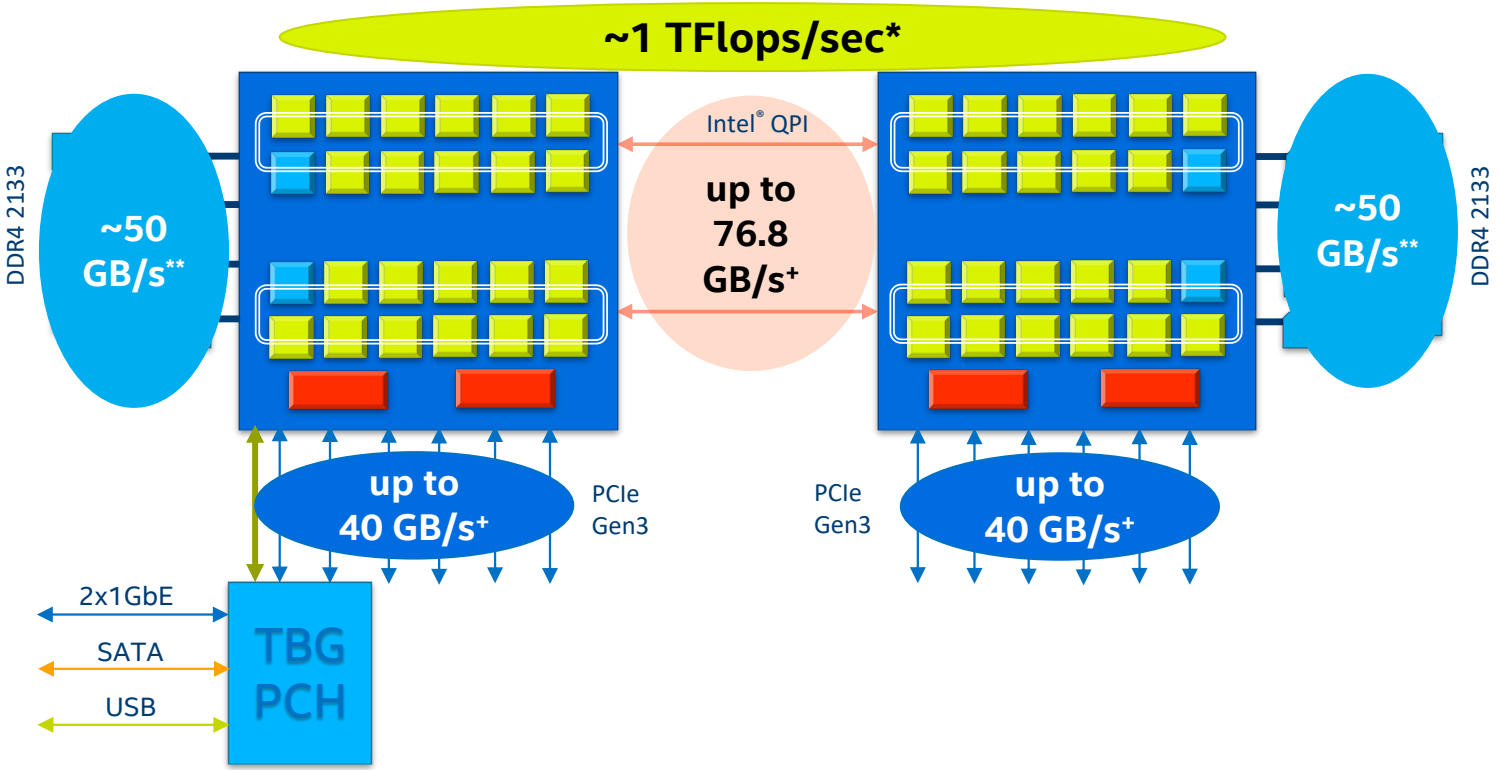
1.65x average gains on HPC workloads comparing Intel® Xeon® Scalable processor to prior generation (geomean of MILC, VASP, OpenFoam, miniFE, LAMMPS).

Intel internal measurements as of June 2018. Configuration details: see backup. * Other names and brands may be claimed as the property of others.

Grantley Platform Performance with Xeon E5-2697 v3



* DGEMM benchmark, ** STREAM Triad benchmark, + peak bandwidth

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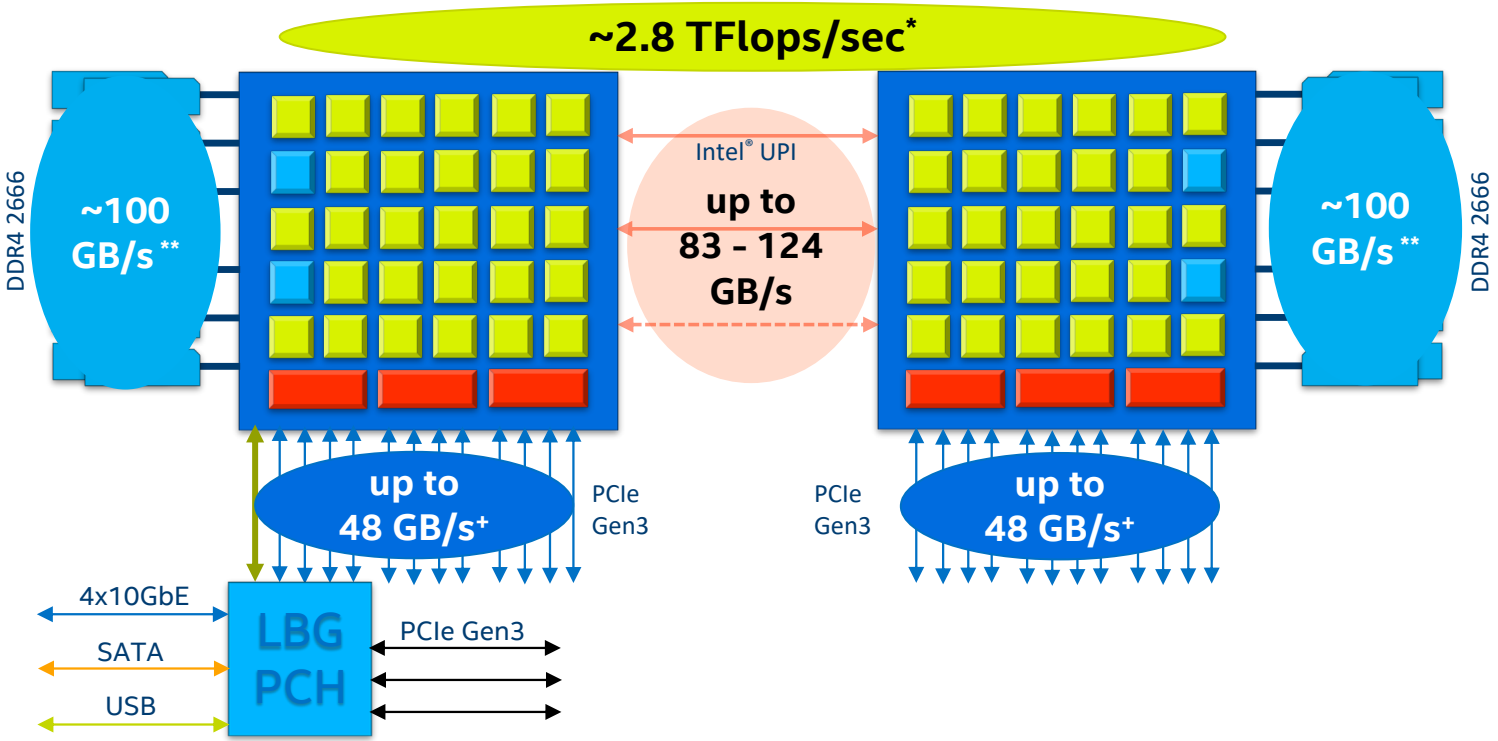
Purley Platform Performance with Xeon Platinum 8174 (205W)



Purley platform delivers up to 2x bandwidth across multiple performance metrics

* DGEMM benchmark, ** STREAM Triad benchmark, + peak bandwidth

Skylake Server Processor Overview

14nm Process Technology with Skylake Core Microarchitecture

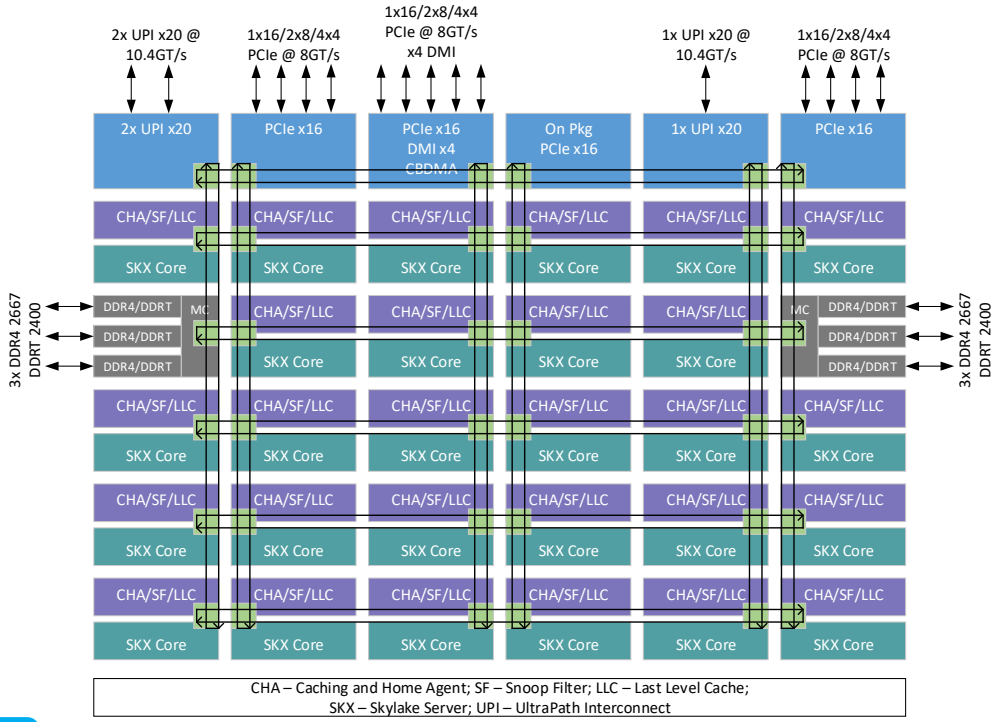
Intel® AVX-512 with 2 FMAs/Core
Virtualization Enhancements
New Memory Protection Features (PPK, MPX, XU/XS)

Rebalanced Cache Hierarchy:
Increased MLC to 1MB/Core
1.375 MB Last Level Cache/Core

Up to 28 Cores on a 2D-Mesh

Intel® Hyper-Threading Technology (2 threads/core)

Intel® Turbo Boost Technology



Power Management:
Per Core P-State (PCPS)
Uncore Frequency Scaling (UFS)
Energy Efficient Turbo (EET)
On die PMAX detection (NEW)
Intel® Speed Shift Technology (NEW)

Memory Technology:
6x DDR4 channels
2133, 2400, 2666 MT/s
RDIMM, LRDIMM

48 Lanes of PCI Express* 3.0
Intel® QuickData Technology Enhancements – 2x bandwidth

Intel® UPI: 10.4GT/s, 30% better eff.

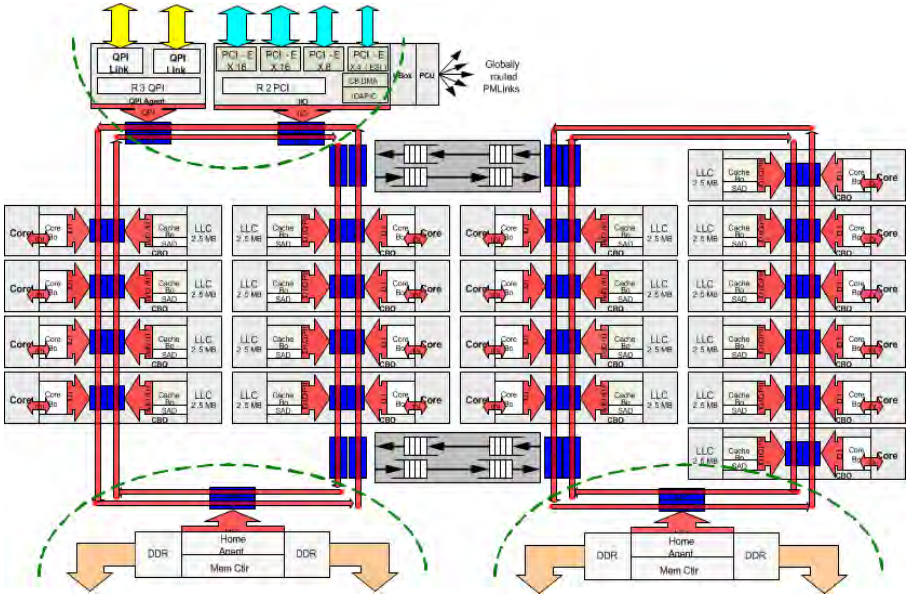
Integrated Voltage Regulator

Existing Feature

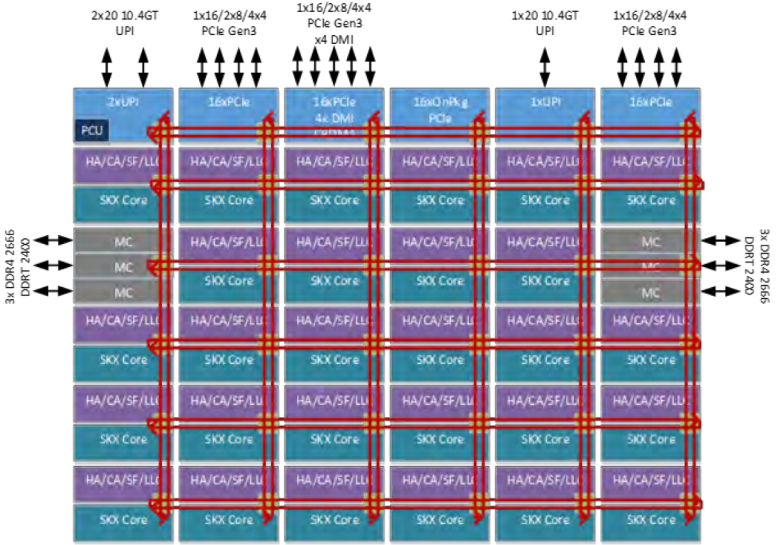
New Skylake Server Feature

New On-Chip Interconnect Architecture

Haswell Server: up to 18 cores per die

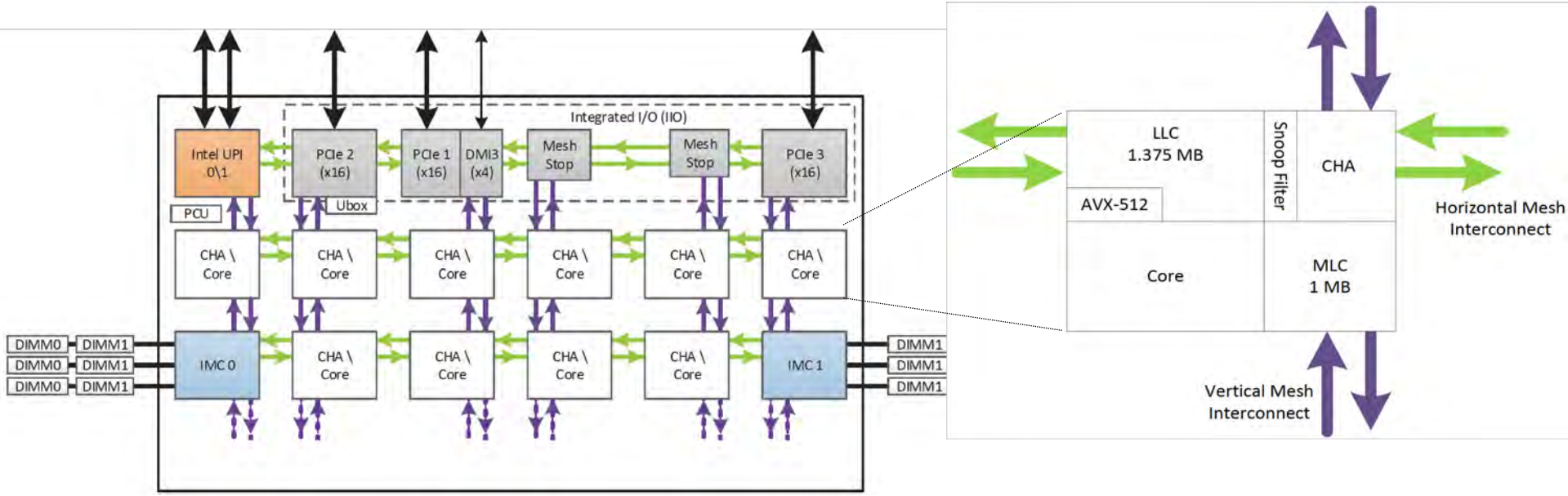


Skylake Server: up to 28 cores per die



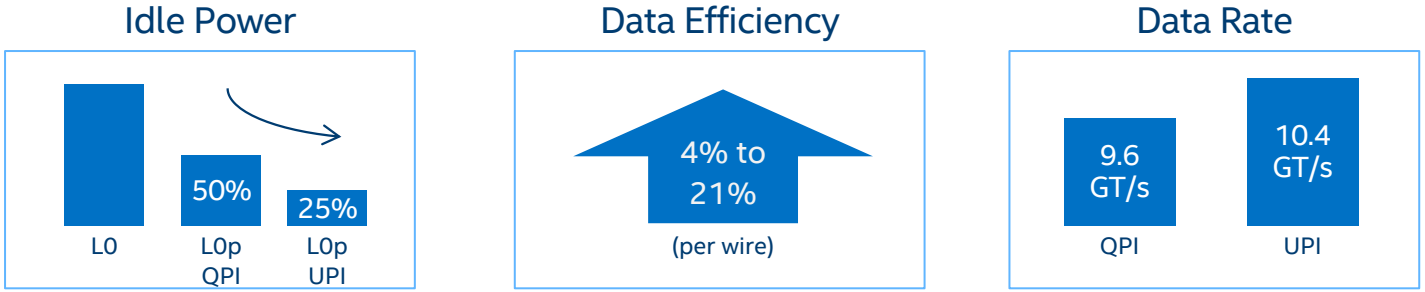
Mesh improves scalability with higher bandwidth and reduced latencies

Skylake Server Socket Diagram



Intel® Ultra Path Interconnect (Intel® UPI)

- Keizer Technology Interconnect (KTI) is now Intel® Ultra Path Interconnect (Intel® UPI), replacing Intel® QPI in the Purley and future platforms
- New, faster coherent link with greater message efficiency
  - Increased bandwidth and performance over QPI
  - Improved messaging efficiency, multiple requests per packet



UPI is not compatible with QPI.
Based on Intel internal measurements

UPI enables high throughput and power efficiency

Coherency Optimizations in Purley Platform

Sub-NUMA Cluster Mode

- Associates LLC slice with nearest memory controller
- Applications use NUMA primitives to achieve lower LLC/memory latency

XPT Prefetch

- Core miss initiates local memory access in parallel with LLC access
- Uses history-based prediction to avoid unnecessary prefetches

UPI Prefetch

- Similar to XPT prefetch, but for UPI requests from remote socket

Local and Remote Direct-to-Core

- Data sent directly from memory controller or UPI to requesting core

Direct-to-UPI

- For UPI requests from remote socket, memory controller directly sends data to UPI instead of going through CHA

UPI Optimizations

- Opportunistic snoop broadcast – avoid directory read to save memory BW
- HitME cache – directory cache for frequently used lines
- IO Directory Cache – directory cache for remote IO writes

Sub-NUMA Clusters (SNC)

Prior generation supported Clusters-On-Die (COD)

SNC provides similar localization benefits as COD, without some of its downsides

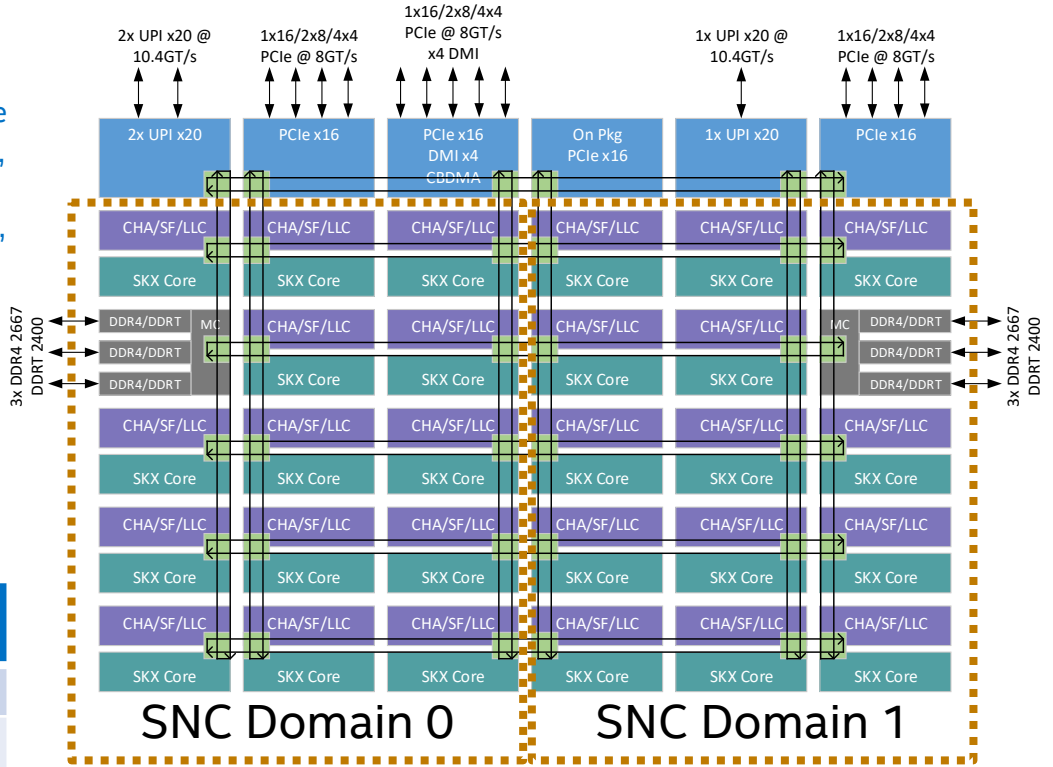
- Only one UPI caching agent required even in 2-SNC mode
- Latency for memory accesses in remote cluster is smaller, no UPI flow
- LLC capacity is utilized more efficiently in 2-cluster mode, no duplication of lines in LLC

Downside with SNC

- Addresses from remote cluster never get cached in local cluster LLC, resulting in larger latency compared to COD in some cases

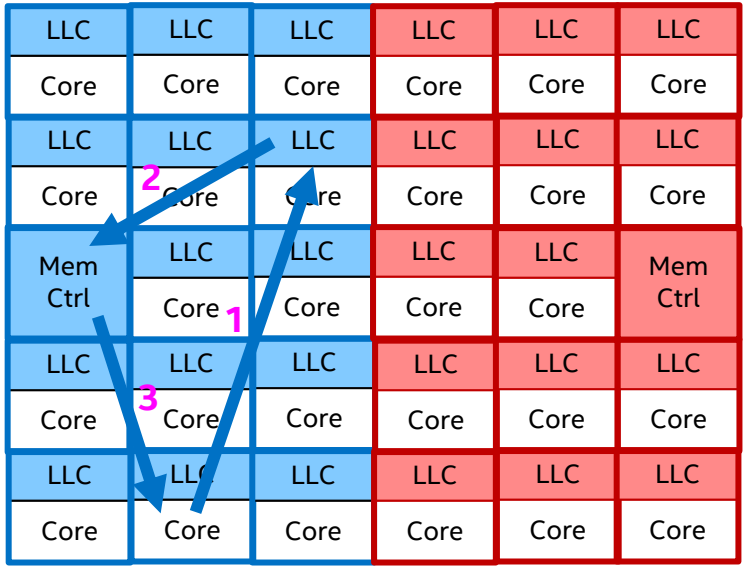
SNC provides extra NUMA node pathways just as COD does. Therefore when setting affinity on Skylake use the same methodology as you would for Haswell/Broadwell

	Clusters per socket	XPT/UPI Prefetch	
SNC off	1	No	No prefetch in UMA
1-SNC	1	Yes	Like SNC off, but can do prefetch
2-SNC	2	Yes	

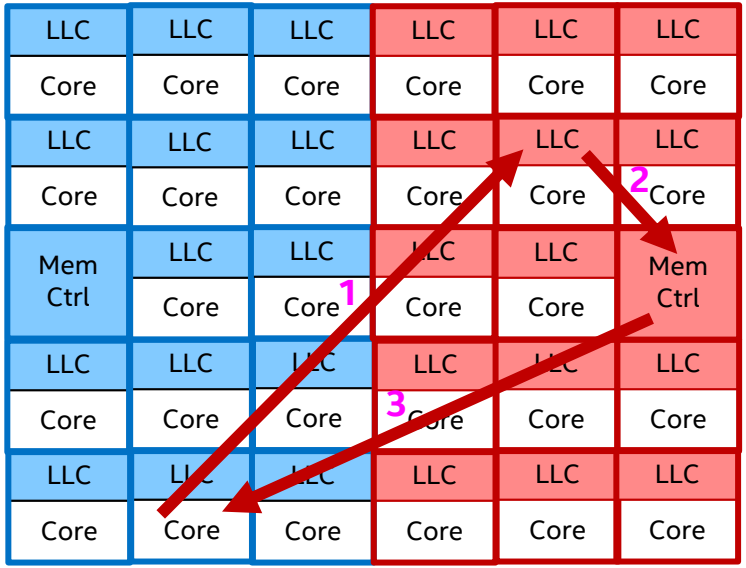


Sub-NUMA Clusters – 2 SNC Example

Local SNC Access

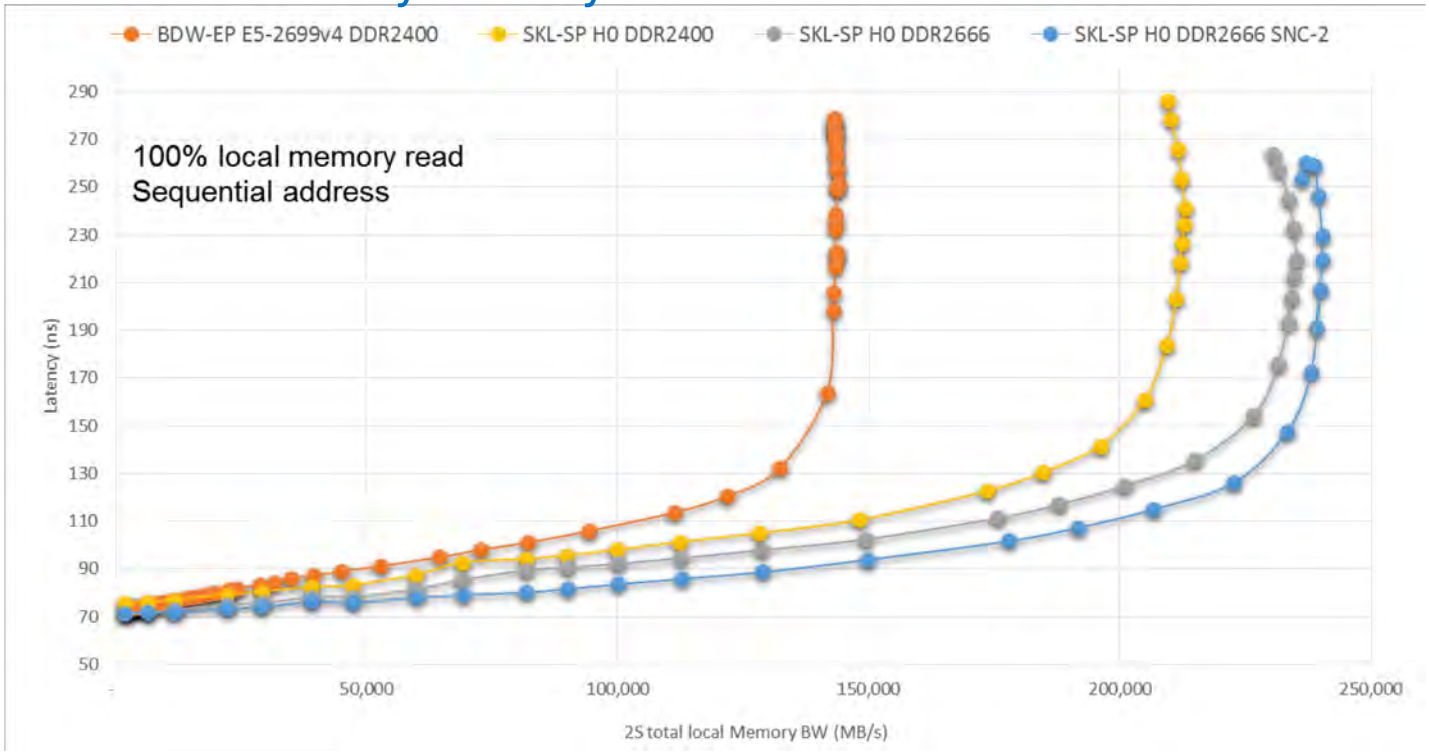


Remote SNC Access



Intel® Xeon® Processor Scalable Family

Dual-socket memory latency & bandwidth*



* Source as of May 2017: Intel internal measurements of BW/latency on platform with Skylake-SP H0 28C internal sample, Core=turbo, CLM=turbo, KTI=10.4, SNC1, 6x32GB DDR4-2400/2667 per CPU, 1 DPC, and platform with E5-2699 v4, Turbo enabled, 4x32GB DDR4-2400, RHEL 7.0. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. **For more information go to http://www.intel.com/performance**

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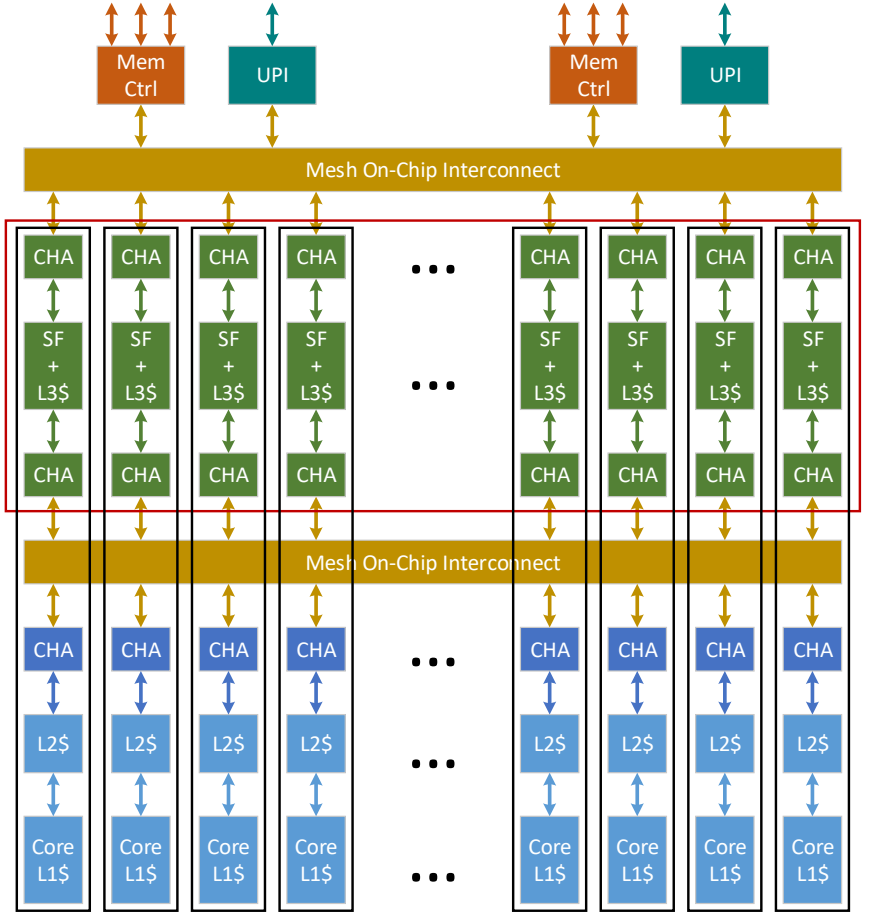
On-Chip Cache Coherency

Distributed LLC or L3 cache – 1.375MB slice physically located with each core

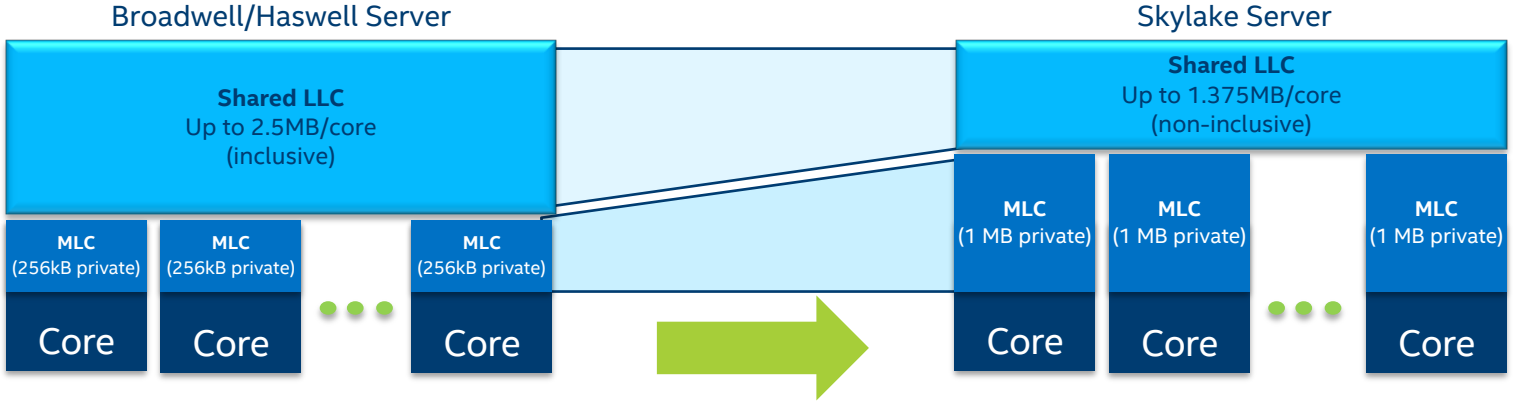
- Cache line address hashed across all L3 slices
- L3 is not inclusive of L2 and L1, acts as victim cache for L2 evictions
- Same L1/L2 tracking capability as SF

Snoop Filter (SF) tracks presence of lines in L2 and L1

- Uses same address hash as L3
- SF+L3 is inclusive of L2 & L1 cache

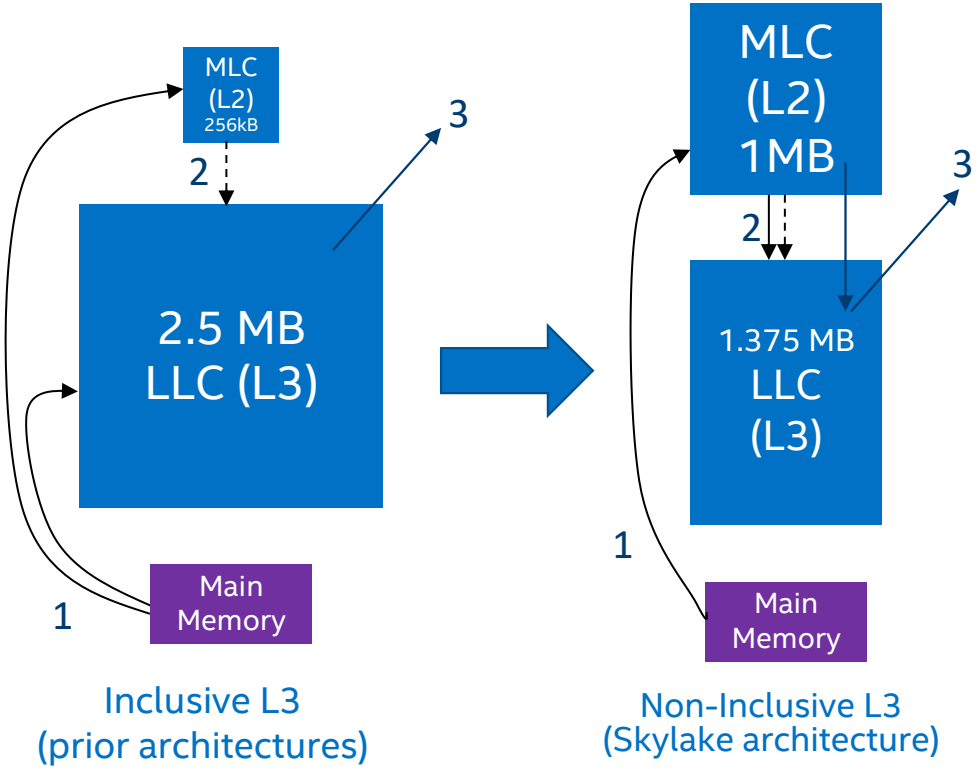


Rebalanced Cache Hierarchy



- Shift cache balance from shared-distributed to private-local by enlarging Mid Level Cache (MLC)
- Shared Last Level cache (LLC) retained to benefit shared data and to enable capacity balancing
- Snoop Filter to track all core owned lines
- Total per Core/LLC tile cache size lower than Broadwell/Haswell
- Higher hit rate on lower latency MLC than Broadwell/Haswell

Inclusive L3 v. Non-Inclusive L3



1. Memory reads fill directly to the MLC, no longer to both the MLC and LLC
2. When a MLC line needs to be removed, both modified and unmodified lines are written back
3. Data shared across cores are copied into the LLC for servicing future MLC misses

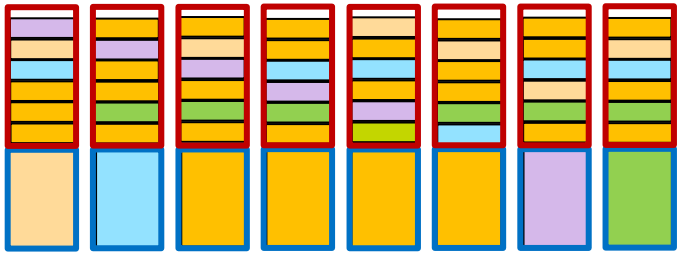
Skylake Server cache hierarchy architected and optimized for server use cases:

- Multithreaded workloads can operate on larger data per thread (due to increased L2 size) and reduce uncore activity
- Virtualized use-cases get larger private L2 cache free from interference

Effect of Cache Rebalancing

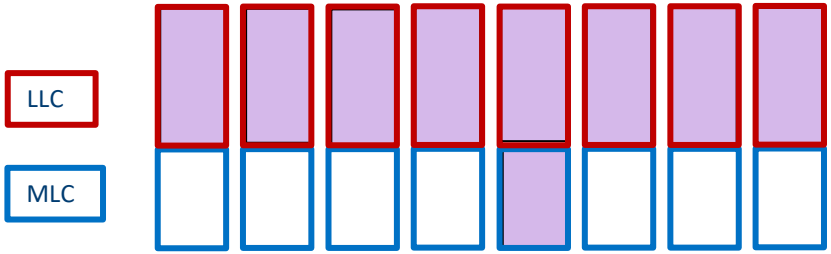
Multi-Threaded, Batch, or Virtualized Workloads

- Effectively utilizes MLC capacity private to each core
- Reduces cache pollution effects from “noisy neighbors”



Single-Thread per socket Workloads

- Does not utilize MLC capacity in the cores not executing the thread
- Larger MLC reduces effective memory latency and performance variability



Concurrent and virtualized workloads effectively utilize available cache capacity

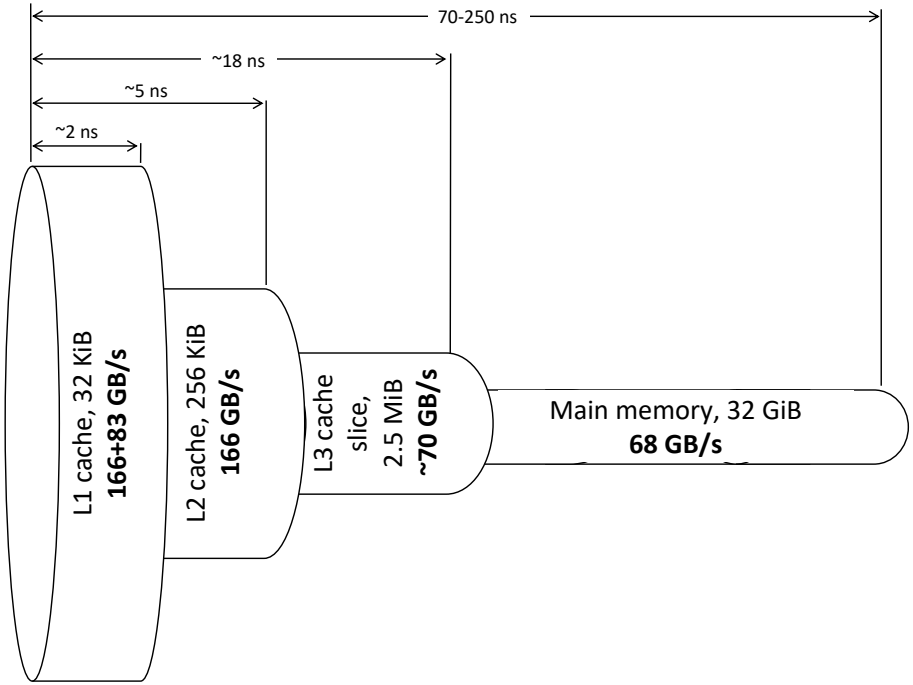
Single thread per socket performance may see some cache capacity deficit

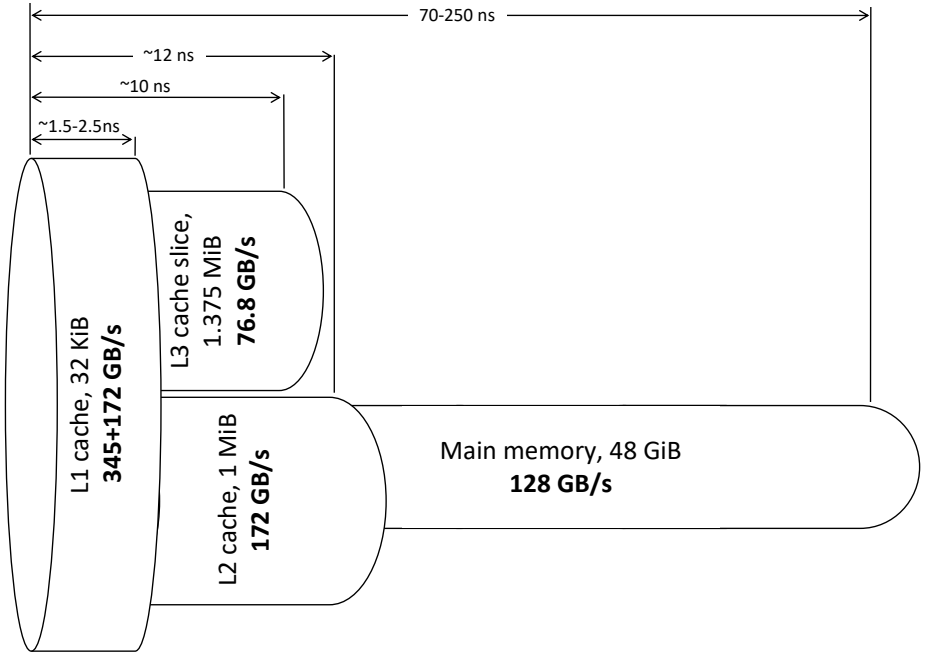
Core Cache Size/Latency/Bandwidth

Metric	Xeon E5 v4 (Broadwell)	Xeon SP (Skylake)
L1 Instruction Cache	32K, 8-way	32K, 8-way
L1 Data Cache	32K, 8-way	32K, 8-way
Fastest Load-to-use	4 cycles	4 cycles
Load bandwidth	64 Bytes/cycle	128 Bytes/cycle
Store bandwidth	32 Bytes/cycle	64 Bytes/cycle
L2 Unified Cache	256K, 8-way	1024K, 16-way
Fastest load-to-use	11 cycles	14 cycles
Bandwidth to L1	64 Bytes/cycle	64 Bytes/cycle
L1 Instruction TLB	4K: 128, 4-way 2M/4M: 8/thread	4K: 128, 4-way 2M/4M: 8/thread
L1 Data TLB	4K: 64, 4-way 2M/4M: 32, 4-way 1G: 4, 4-way	4K: 64, 4-way 2M/4M: 32, 4-way 1G: 4, 4-way
L2 Unified TLB	4K+2M shared: 1536, 12-way 1G: 16 entries	4K+2M shared: 1536, 12-way 1G: 64 4-way entries

Note: Red = Differences

Memory hierarchy evolution summary





Based on Intel engineering estimates. Diagrams scale not representing actual metric values.

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High-Level Skylake Core Microarchitecture Improvements

Improved front-end

- Improved and larger Branch Predictor
- Wider and Deeper Instruction Supply

Deeper Out-of-Order Buffers

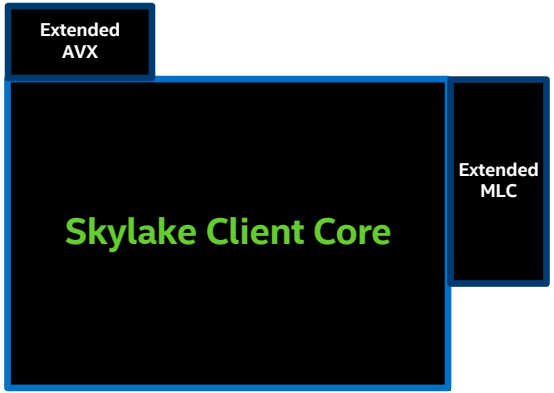
- Extract more instruction parallelism

More execution units, shorter latencies

- Improved Divider (Radix1024), 2x 128 bit

More Load/Store Bandwidth than BDW

- Prefetcher improvements
- Deeper store buffer, fill buffer and WB buffer
- Higher bandwidth



Expandable core for datacenter specific enhancements

- Second AVX-512 FMA
- Larger 1MB MLC

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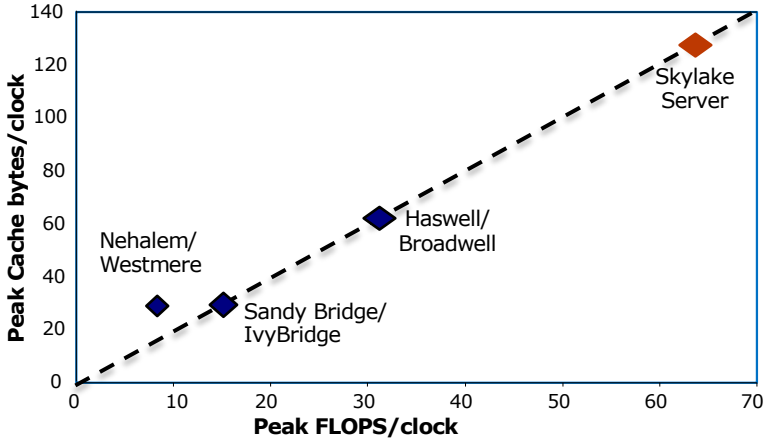
Skylake Server Peak FLOPS



uArch	Instruction Set	SP FLOPs per cycle	DP FLOPs per cycle
Nehalem	SSE (128-bits)	8	4
Sandy Bridge	AVX (256-bits)	16	8
Haswell / Broadwell	AVX2 & FMA	32	16
Skylake Server	AVX512 & FMA	64	32

Skylake Server Peak Compute Throughput

- AVX-512 with 2 FMAs per core provide 2x peak FLOPs/cycle of Haswell/Broadwell
- 2x cache bandwidth to feed wider vector units
  - 64-byte load/store from L1
  - 2x L2 bandwidth

Intel® AVX-512 Instruction Types	
AVX512-F	AVX-512 Foundation Instructions
AVX512-VL	Vector Length Orthogonality : ability to operate on sub-512 vector sizes
AVX512-BW	512-bit Byte/Word support
AVX512-DQ	Additional D/Q/SP/DP instructions (converts, transcendental support, etc.)
AVX512-CD	Conflict Detect : used in vectorizing loops with potential address conflicts

Based on Intel engineering estimates.

Intel® Advance Vector Extensions 512 (AVX-512)

Intel® AVX (Sandy Bridge & Ivy Bridge)	Intel® AVX2 (Haswell & Broadwell)	Intel® AVX-512 (Skylake-SP)
• 16 SP/8 DP Flops/Cycle • 256-bit basic FP • 16 registers • NDS (and AVX128) • Improved blend • MASKMOV • Implicit unaligned	• 32 SP/16 DP Flops/Cycle • Float16 • 2 256-bit FP FMAs (Fused Multiply-Add) • 256-bit integer • PERMD • Gather	• Up to two 512-bit FMAs • 512-bit FP and Integer • 32 registers • 8 mask registers • 64 SP/32 DP Flops/Cycle (SKUs with 2 512-bit FMAs) • 32 SP/16 DP Flops/Cycle (SKUs with 1 512-bit FMA) • Embedded rounding • Embedded broadcast • Scalar/SSE/AVX “promotions” • Native media additions • HPC additions • Transcendental support • Gather/Scatter

AVX512 features

Higher throughput

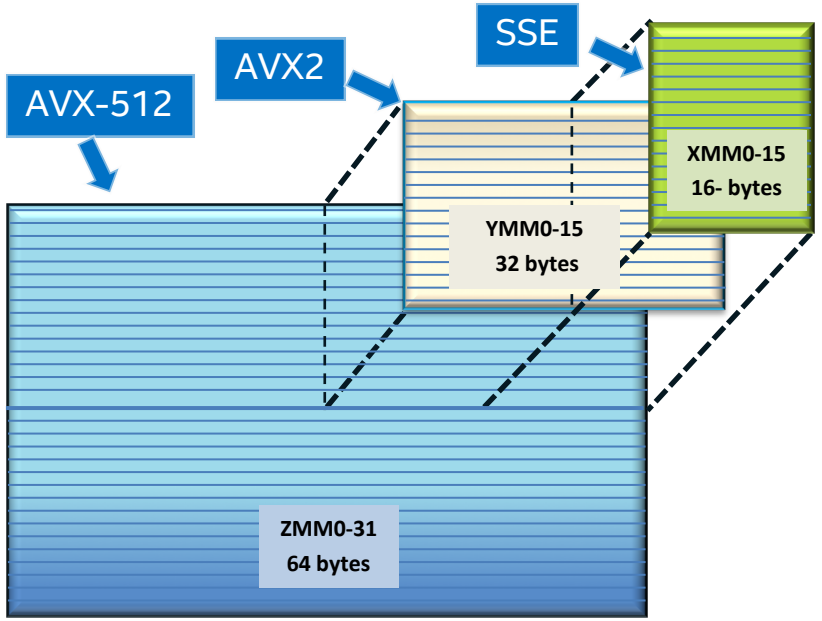
Greatly improved unrolling and inlining opportunities

32 vector registers, 512b wide: zmm0 through zmm31

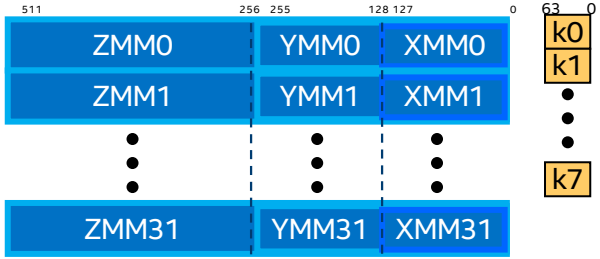
- Overlaid on top of existing YMM arch state
- Writing to xmm zeroes bits [511:128]
- writing to ymm zeroes bits [511:256]

8 mask registers, 64b wide: k0 through k7

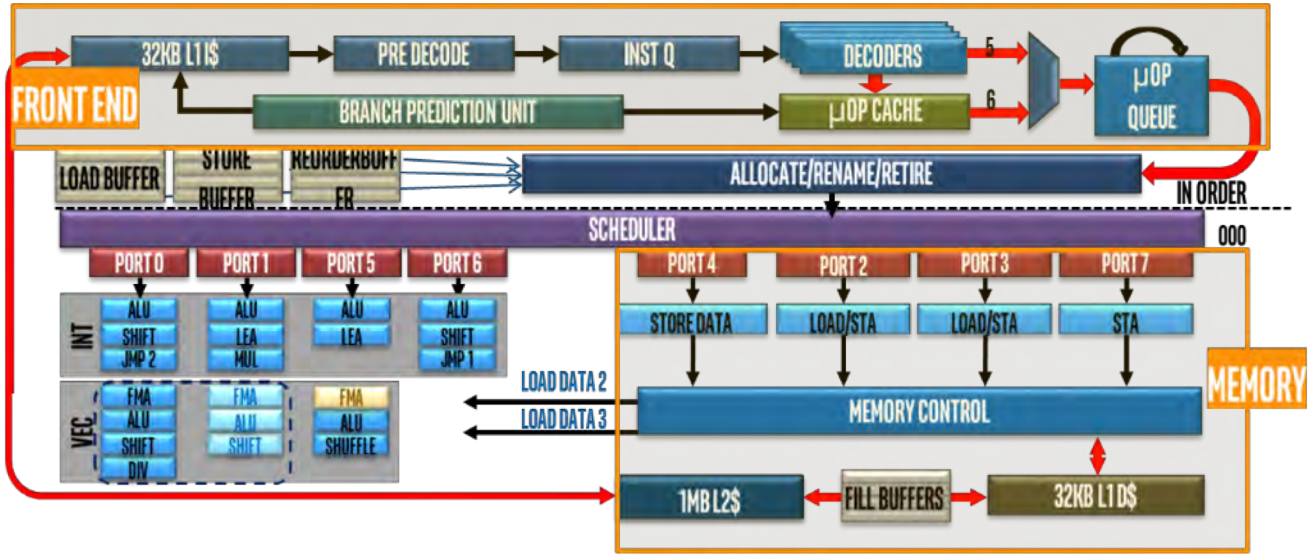
- KNL only uses bits [15:0] though (PS,PD,D,Q)
- EVEX.aaa=000 is an indicator of “no mask”
  - {k0} is illegal



	Skylake Server	Xeon Phi Knights Landing
AVX-512 foundation (F)	Yes	Yes
AVX-512 conflict detection (CDI)	Yes	Yes
AVX-512 exponential and reciprocal (ERI)	No	Yes
AVX-512 prefetch (PFI)	No	Yes
AVX-512 Byte and Word Instructions (BW)	Yes	No
AVX-512 Doubleword and Quadword Instructions (DQ)	Yes	No
AVX-512 Vector Length Orthogonality (VL)	Yes	No



Skylake Core Microarchitecture Enhancements



	Broadwell uArch	Skylake uArch
Out-of-order Window	192	**224**
In-flight Loads + Stores	72 + 42	72 + **56**
Scheduler Entries	60	**97**
Registers – Integer + FP	168 + 168	**180** + 168
Allocation Queue	56	**64/thread**
L1D BW (B/Cyc): Load+Store	64 + 32	**128** + **64**
L2 Unified TLB	4K+2M: 1024	4K+2M: **1536** **1G: 64**

Larger and improved branch predictor, higher throughput decoder, larger window

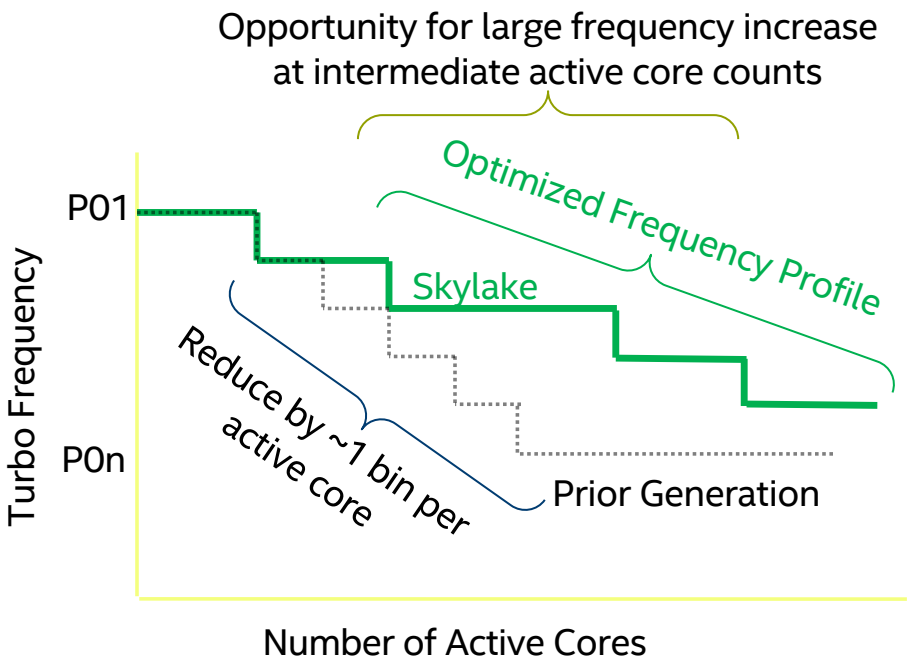
Improved scheduler and execution engine, improved throughput and latency of divide/sqrt

More load/store bandwidth, deeper load/store buffers, improved prefetcher

Server specific enhancements ➔ 2nd 512-bit FMA, larger 1MB L2 per core (vs. 256KB per core for client core)

Skylake microarchitecture delivers ~10% (geomean) IPC improvement vs. Broadwell

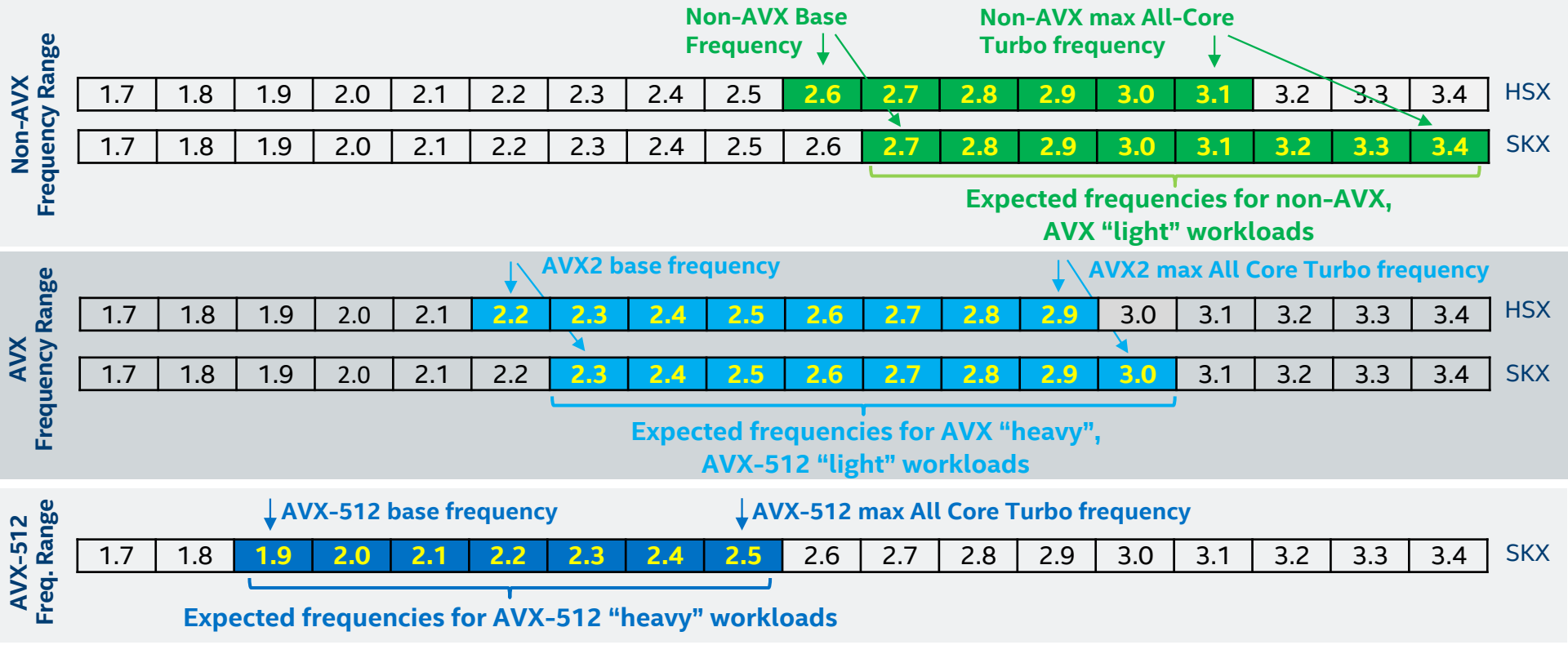
New Optimized Turbo Profiles



- Prior generation server CPUs typically decreased frequencies by 1 bin for each additional active core
- Skylake server processor reduces frequencies more gradually as the number of active cores increases

Processor Frequency for SSE & AVX workloads

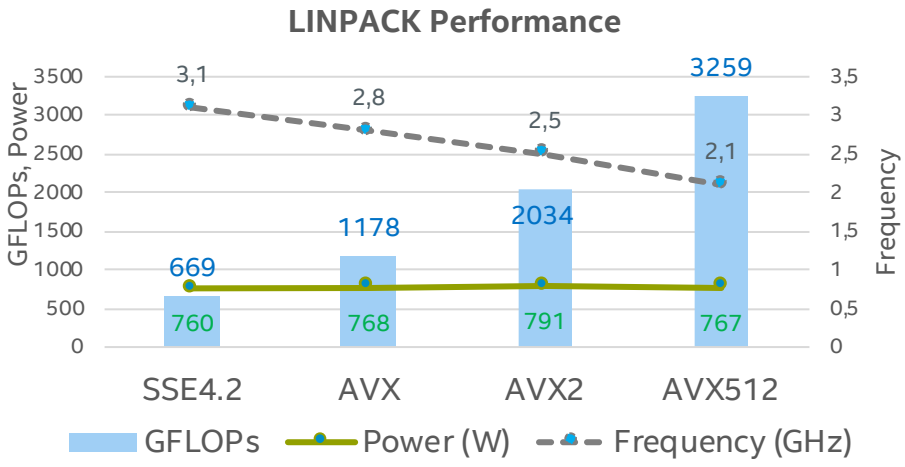
Intel Xeon E5-2697 v3 and Intel Xeon Platinum 8174 Processor at 205W TDP used for illustration purposes

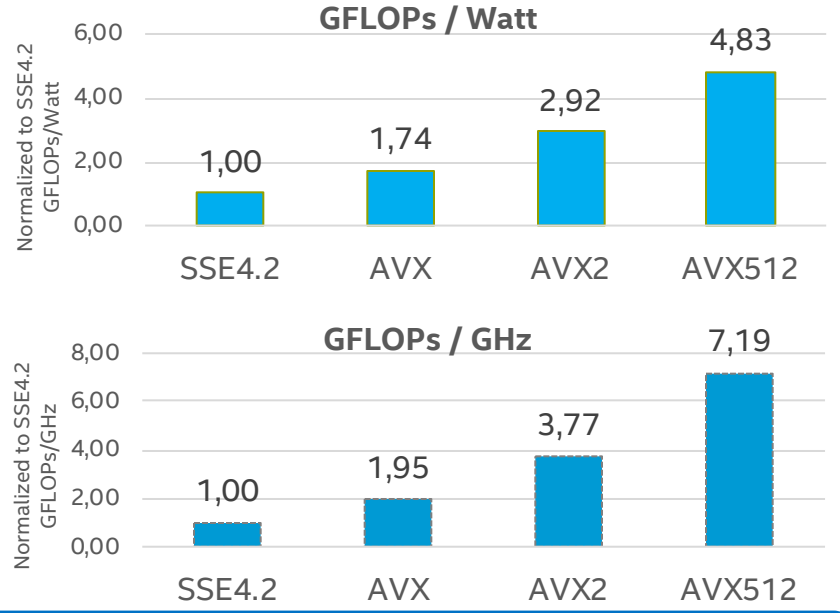


Source: Intel® Xeon® Processor E5 v3 Product Family Specification Update (https://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/xeon-e5-v3-spec-update.pdf) and Intel® Xeon® Processor Scalable Specification Update (https://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/xeon-scalable-spec-update.pdf)

AVX-512 “Heavy” Usage Examples

Significant gains for vector workloads while balancing power and frequency





Intel® AVX is designed to balance power consumed by lowering frequency when needed, while delivering significant performance gains and reduced runtimes

Performance estimates were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. Configuration Summary: 1-Node, 2 x Intel® Xeon® Platinum 8180 Processor on Purley-EP (Lewisburg) (S2600WF) with 1584 GB (12x32GB DDR4-2666) Total Memory, Intel S3610 800GB SSD, BIOS: SE5C620.86B.01.00.0471.040720170924, 04/07/2017, RHEL Kernel: 3.10.0-514.16.1.el7.x86_64 x86_64,

Benchmark: Intel® Optimized MP LINPACK - Higher is better

Basic software tools enabling Skylake support

Compiler

- Targeting AVX512 ISA:
  `-xCORE-AVX512`
  `-xSKYLAKE` or `-xSKYLAKE-AVX512`
  -mtune=skylake or -mtune=skylake-avx512
- Controlling 512-bit register usage with `-qopt-zmm-usage=<keyword>`
  `high` - generate zmm code without restrictions
  `low` – tell compiler that is should avoid using 512-bit wide registers

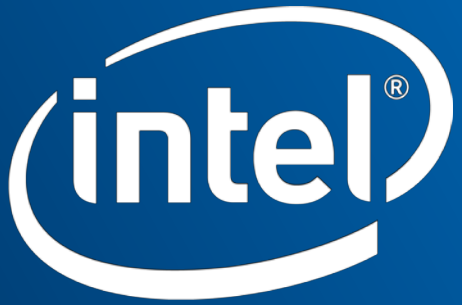
Intel MPI Library

`I_MPI_PLATFORM=skx`
`I_MPI_SHM=[skx_avx512 | skx_avx2 | skx_sse]`
with `I_MPI_FABRICS=shm:ofi`

Purley/Skylake Call To Action

The Skylake family of server processors brings amazing performance on demanding workloads

- Take advantage of Intel® AVX-512 on Intel® Compiler 19.0+ and Parallel Studio XE 2019 Update 3
- Take advantage of new larger mid-level cache size for reduced latency and higher core count for improved parallelism
- Explore localization benefits such as reduced latency for memory accesses and an increase in efficiency of the LLC due to elimination of duplicate cache lines


intel®

Skylake Cache Hierarchy

	L1-I	L1-D	L2 (MLC)	Snoop Filter Slice	L3 (LLC) Slice	Directory in memory
Line Size (B)	64	64	64	N/A	64	2-bits/line
Sets	64	64	1024	2048	2048	N/A
Associativity	8-way	8-way	16-way	12-way	11-way	N/A
Cache Size	32KB	32KB	1MB	Eqv. 1.5MB	1.375MB	N/A
Latency (Cyc)	N/A	4	14	Variable	Variable	Variable
Peak BW (B/Cyc)	N/A	128+64	64	N/A	32	N/A
Inclusivity	N/A	N/A	L1-I, L1-D	All L2s & IO	Non-incl	All L2 & L3
Fill Policy	On a miss			On a miss	L2 Evict	N/A
Update Policy	N/A	Writeback		N/A	Writeback	N/A
States	I, V	M/E/S/I	M/E/S/I	M/E/S/I, CV bits	M/E/S/I	I/A/S

Configurations: High Performance Compute Apps

Intel® Xeon® Scalable Processor

Performance results are based on testing as of June 2018 and may not reflect all publicly available security updates. See configuration disclosure for details. No product can be absolutely secure.
Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit www.intel.com/benchmarks. Configuration details:

7. 1.6X average gains on HPC workloads comparing Intel® Xeon® Scalable processor to prior generation (geomean of MILC, VASP, OpenFoam, YASK iso3dfd, miniFE, LAMMPS, DGEMM). Intel internal measurements as of June 2018: 1-node, 2-sockets of Intel® Xeon® Gold 6148, Platform: Wolf Pass / S2600WF/H48104-850, Memory configuration: 12 slots / 16 GB/ 2666 MT/s DDR4 RDIMM, Total Memory per Node: 192, Hyper-Threading: Yes, Turbo: Off, ucode: x043, OS: Red Hat Enterprise Linux* 7.4, Kernel: 3.10.0-693.11.6.el7.x86_64, Score: [MILC= 57.4 GFLOPs/sec, VASP=116.1 sec, OpenFoam=553, miniFE=30.4 Gflops, LAMMPS=74, DGEMM=2231.9Gflops] vs. 1-node, 2-sockets of Intel® Xeon® E5-2699 v4, Platform: Grantley / S2600WTT/H48298-300, Memory configuration: 8 slots / 16 GB/ 2400 MT/s DDR4 RDIMM, Total Memory per Node: 128, HyperThreading : Yes, Turbo: Off, ucode: 0x02A, OS: Red Hat Enterprise Linux* 7.4, Kernel: 3.10.0-693.21.1.el7.x86_64, Score: [MILC=40 Gflops/sec, VASP= 209.4 sec, OpenFoam=879.4, miniFE=19.3Gflops, LAMMPS=33.3, DGEMM=1413 Gflops]

1c. Up to 1.55x on integer throughput performance - estimates based on Intel internal testing as of June 2018 on SPECint*_rate_base2006 : 1-Node, 2 x Intel® Xeon® Platinum 8180M Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: SPEC CPU® 2017, Compiler: Intel® Compiler IC18 OEM, Optimized libraries: AVX512. ucode: 0x043, Data Source: Request Number: 40, Benchmark: SPECrate*2017_int_base, Score: 281 Higher is better vs. 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Wildcat Pass with 256 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: SPEC CPU® 2017 v1.2, Optimized libraries: IC18.0_20170901, Other Software: MicroQuill SMART HEAP, Script / config files : xCORE-AVX2. ucode: 0x02A, Data Source: Request Number: 40, Benchmark: SPECrate*2017_int_base, Score: 181 Higher is better

1d. Up to 1.55x on technical compute app throughput - estimates based on Intel internal testing as of June 2018 on SPECfp*_rate_base2006: 1-Node, 2 x Intel® Xeon® Platinum 8180M Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: SPEC CPU® 2017, Compiler: Intel® Compiler IC18 OEM, Optimized libraries: AVX512. ucode: 0x043, Data Source: Request Number: 39, Benchmark: SPECrate*2017_fp_base, Score: 236 Higher is better vs. 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Wildcat Pass with 256 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: SPEC CPU® 2017 v1.2, Optimized libraries: IC18.0_20170901, Other Software: MicroQuill SMART HEAP, Script / config files : xCORE-AVX2. ucode: 0x02A, Data Source: Request Number: 39, Benchmark: SPECrate*2017_fp_base, Score: 148 Higher is better

1e. Up to 1.6x on est STREAM - triad - estimates based on Intel internal testing as of June 2018 on STREAM - triad: 1-Node, 2 x Intel® Xeon® Platinum 8180M Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: STREAM , Compiler: Intel® Compiler IC17, Optimized libraries: AVX512. ucode: 0x043, Data Source: Request Number: 37, Benchmark: STREAM - Triad, Score: 201.24 Higher is better vs. 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Wildcat Pass with 256 GB Total Memory on Red Hat Enterprise Linux* 7.4 using Benchmark software: STREAM, Optimized libraries: IC16, Other Software: AVX2. ucode: 0x02A, Data Source: Request Number: 37, Benchmark: STREAM - Triad, Score: 124.78 Higher is better

1i. Up to 2.2x Linpack throughput - estimates based on Intel internal testing as of June 2018 on Intel® Distribution of LINPACK: 1-Node, 2 x Intel® Xeon® Platinum 8180M Processor on Wolf Pass SKX with 384 GB Total Memory on Red Hat Enterprise Linux* 7.4 OS Kernel: 3.10.0-693.11.6.el7.x86_64, Update uCode: 0x043 using Benchmark software: MP Linpack 2018.0.006, Compiler: l_mpi_2018.1.163, Optimized libraries: AVX512, Array 80000. Data Source: Request Number: 38, Benchmark: Intel® Distribution of LINPACK, Score: 3367.5 Higher is better vs. 1-Node, 2 x Intel® Xeon® Processor E5-2699 v4 on Wildcat Pass with 256 GB Total Memory on Red Hat Enterprise Linux* 7.4 OS Kernel: 3.10.0-693.21.1.el7.x86_64 , uCode: 0x02A using Benchmark software: MP Linpack 2018.0.006, Optimized libraries: l_mpi_2018.1.163, AVX2, Array 80000, Other Software: MicroQuill SMART HEAP, Script / config files : xCORE-AVX2. Benchmark: Intel® Distribution of LINPACK, Score: 1427.23 Higher is better