# Back to the Root of Timing

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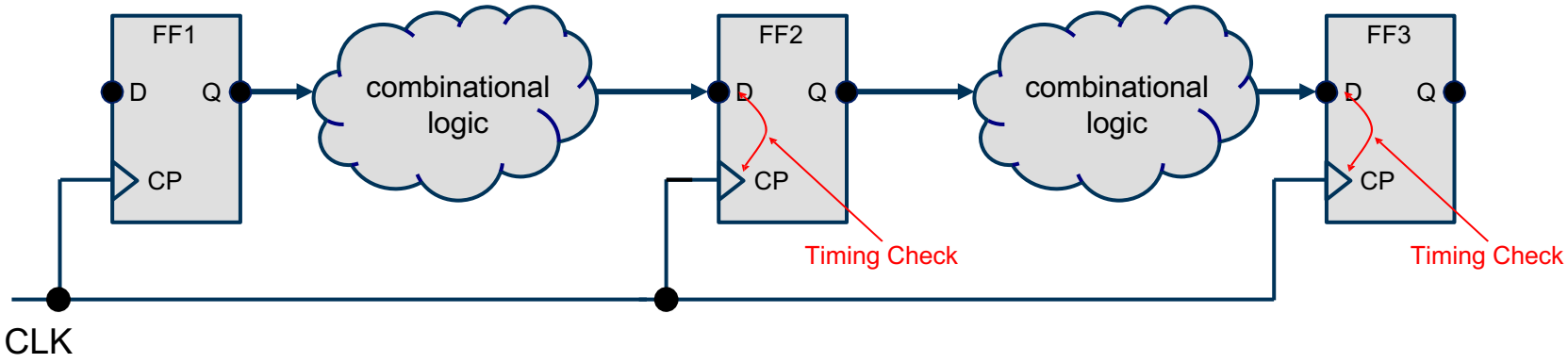
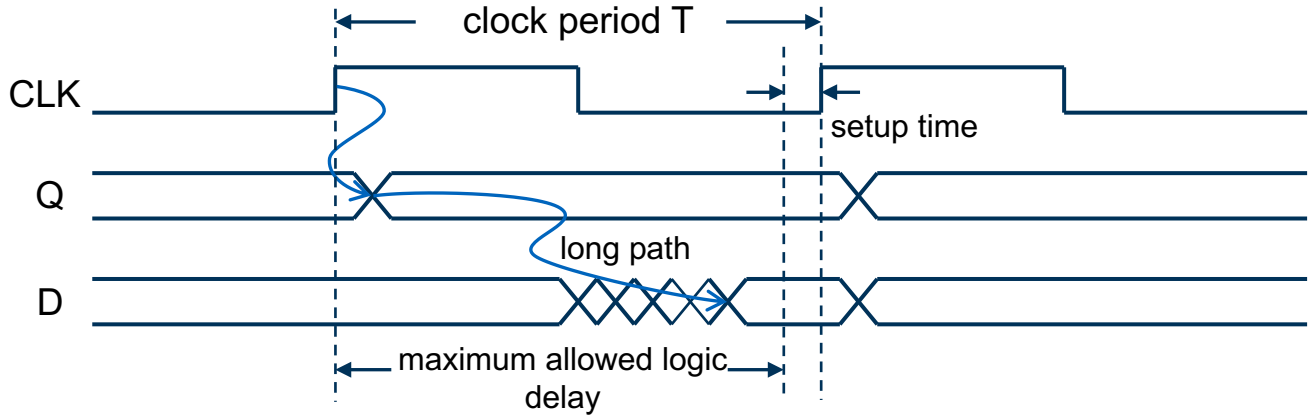
Chair of Electronic Design Automation

# Digital Circuits

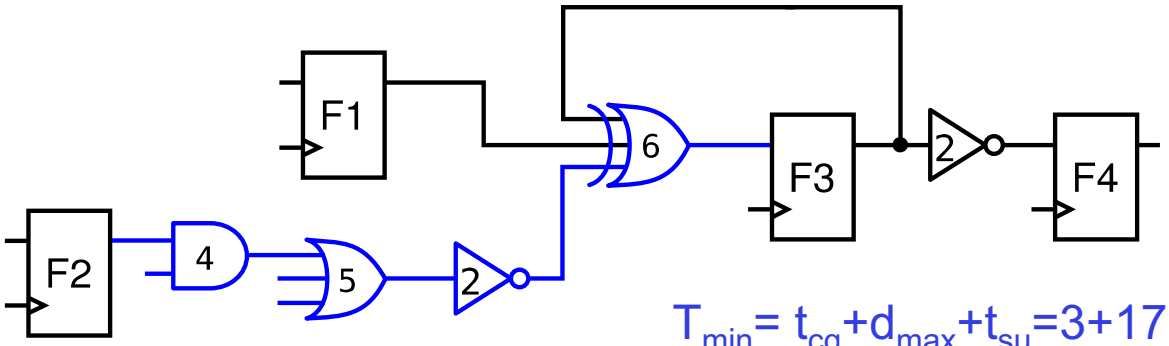



- **Combinational logic blocks** perform computation.
- **Sequential components** such as flip-flops synchronize signal propagation.
- **Timing constraints** should be checked at flip-flops.

# Timing of Digital Circuits




The delays of the longest paths determine the minimum clock period and thus the maximum clock frequency.




Clock-to-q delay $t_{cq}$: 3
Setup time $t_{su}$: 1

$T_{min} = t_{cq} + d_{max} + t_{su} = 3 + 17 + 1 = 21$

# Clock Frequencies: ITRS 2004 and 2013

ITRS (International Technology Roadmap for Semiconductors) 2004

| *Year of Production* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* | *2016* | *2017* | *2018* |
|---|---|---|---|---|---|---|---|---|---|
| *Technology Node* | *hp45* | | | *hp32* | | | *hp22* | | |
| *Chip Frequency (MHz)* | | | | | | | | | |
| *On-chip local clock* | **15,079** | | **20,065** | **22,980** | | **33,403** | **39,683** | | **53,207** |

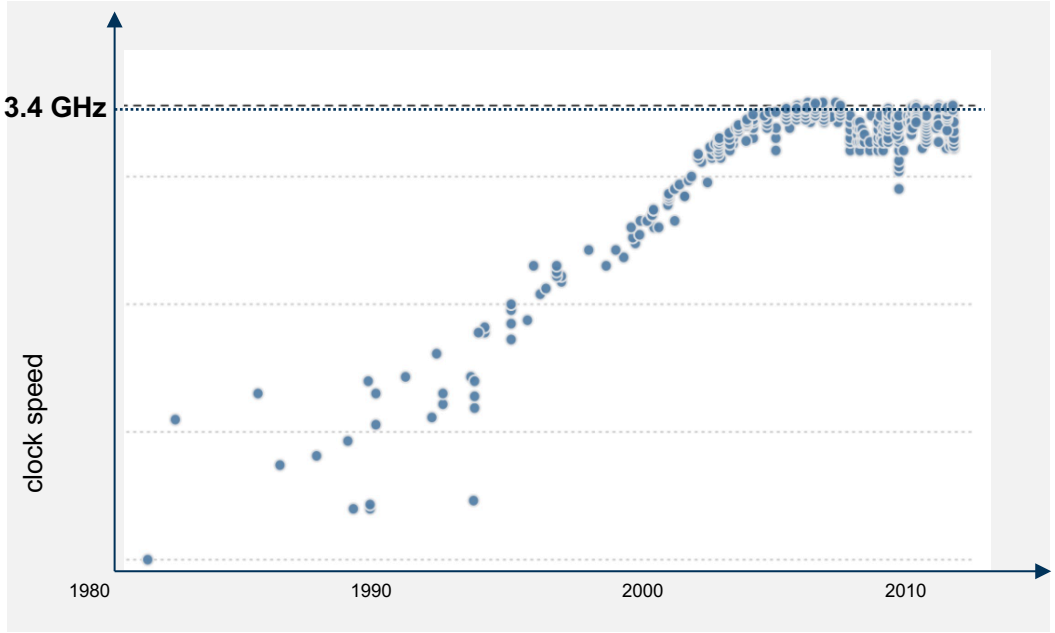
Clock frequency doubles every 3 years

ITRS 2013

| *Year of Production* | *2013* | *2015* | *2017* | *2019* | *2021* | *2023* | *2025* | *2028* |
|---|---|---|---|---|---|---|---|---|
| *Logic Industry "Node Name" Label* | "16/14" | "10" | "7" | "5" | "3.5" | "2.5" | "1.8" | |
| On-chip local clock MPU HP [at 4% CAGR] | 5.50 | 5.95 | 6.44 | 6.96 | 7.53 | 8.14 | 8.8 | 9.9 |

Clock frequency doubles every 15 years

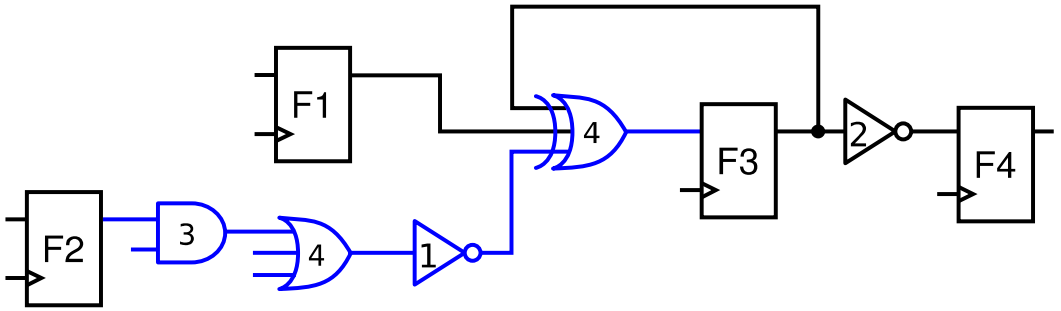
# Trend of CPU Frequencies


Stagnation in single-core CPU clock frequency
[Colin Gillespie, 2016]

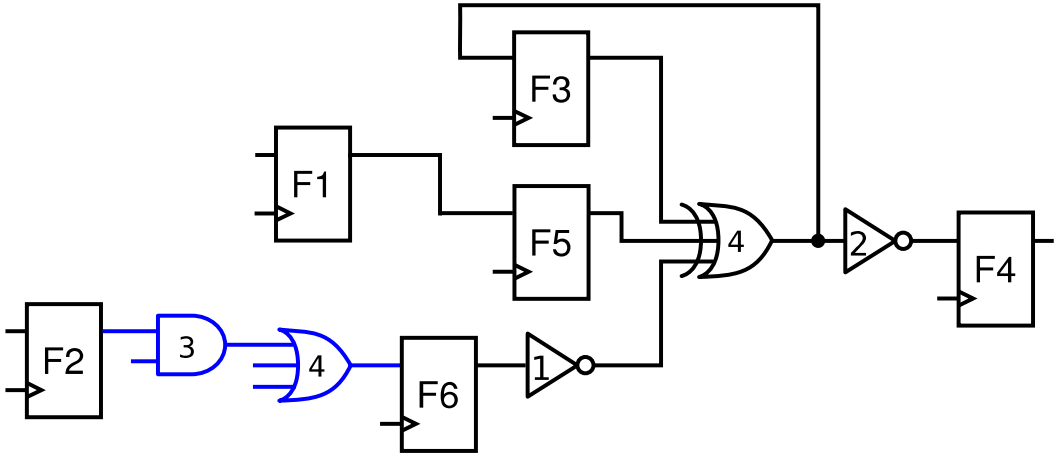
# Timing Optimization Methods

**Gate Sizing**




$T_{min}$=3+12+1=16

**Retiming**



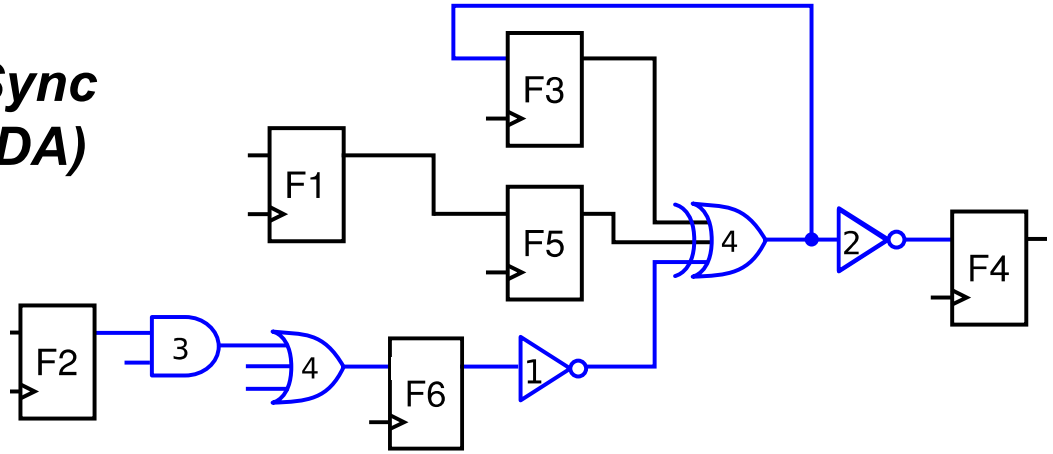

$T_{min}$=3+7+1=11

The limit in the traditional timing paradigm

- Delay imbalances between flip-flop stages degrade performance
- Flip-flops have clock-to-q delays and impose setup time.

# The Root of Timing

***VirtualSync (TUM-EDA)***



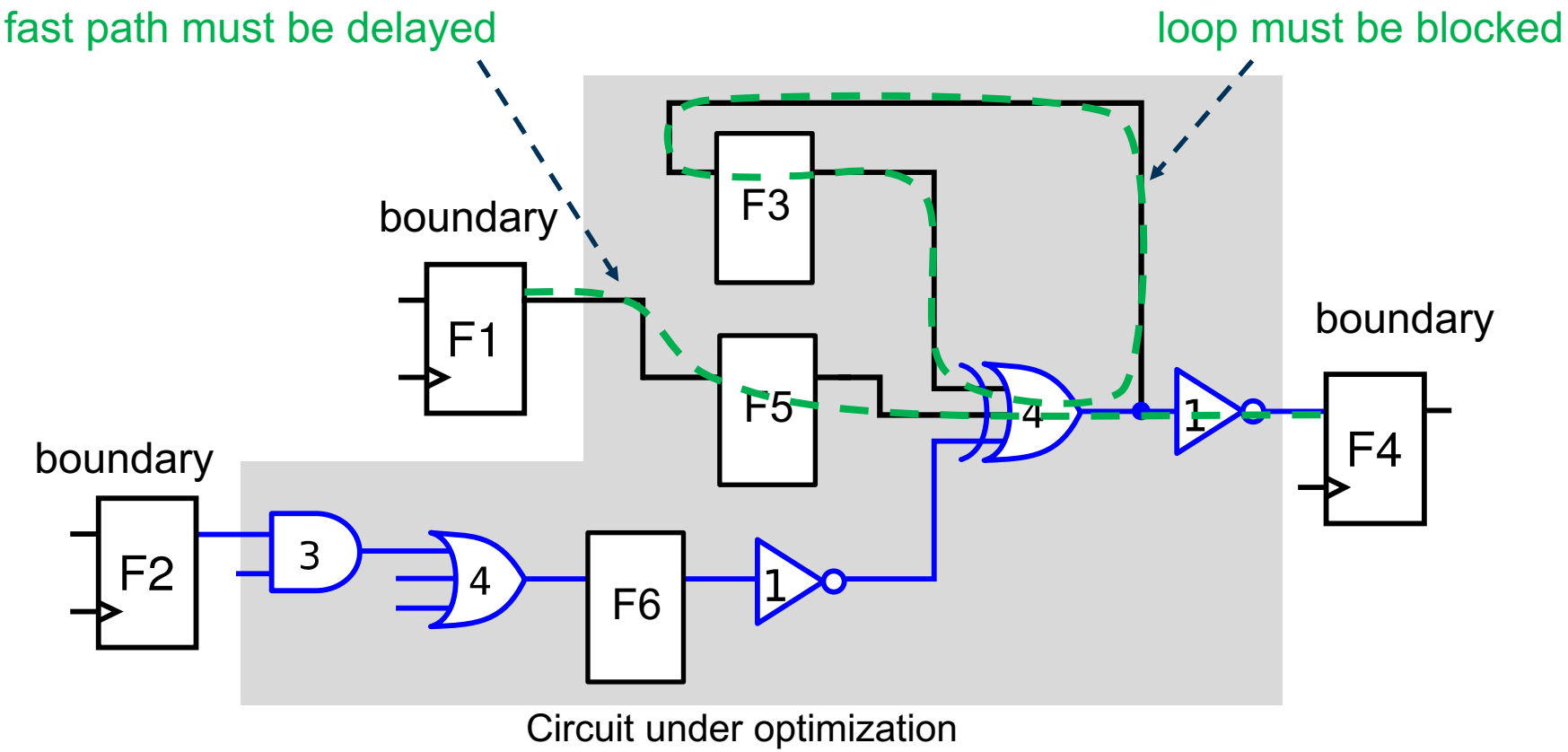

$T_{min}$=(3+13+1)/2=8.5

22.7% reduction compared with retiming&sizing

With $T_{min}$, the signal from F2 reaches F3 and F4 after the first clock edge and before the second clock edge.

- States of the circuit: Snapshots of signal values at internal circuit nodes.
- Signals arrive at boundary flip-flops correctly without flip-flops → Virtual Synchronization (VirtualSync).
- Synchronizing signal propagations **with flip-flops** is not always necessary.

# VirtualSync Concept

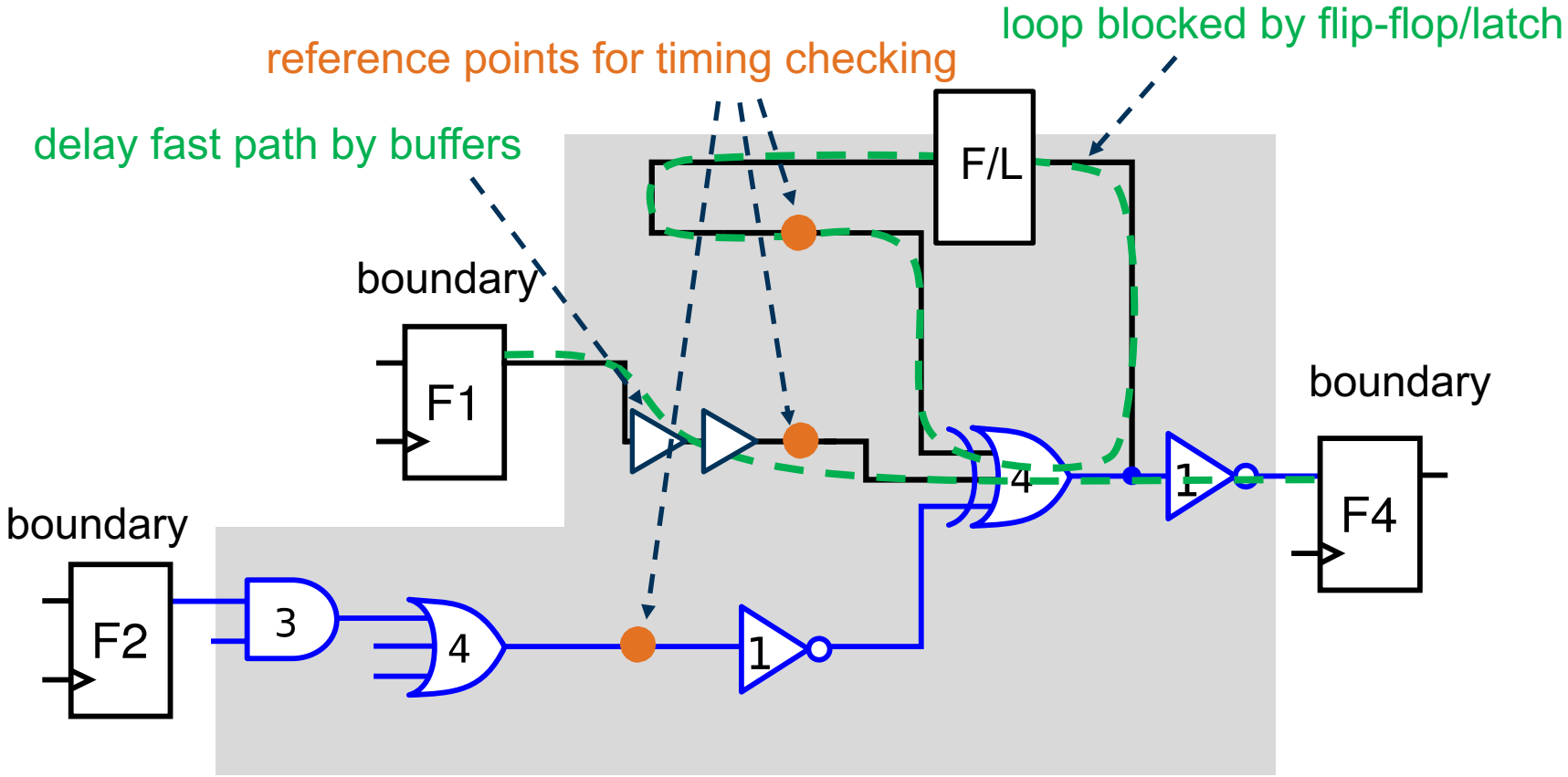



Step 1: Remove all flip-flops except those at the boundary of the module

Step 2: Block fast signals for timing synchronization, including

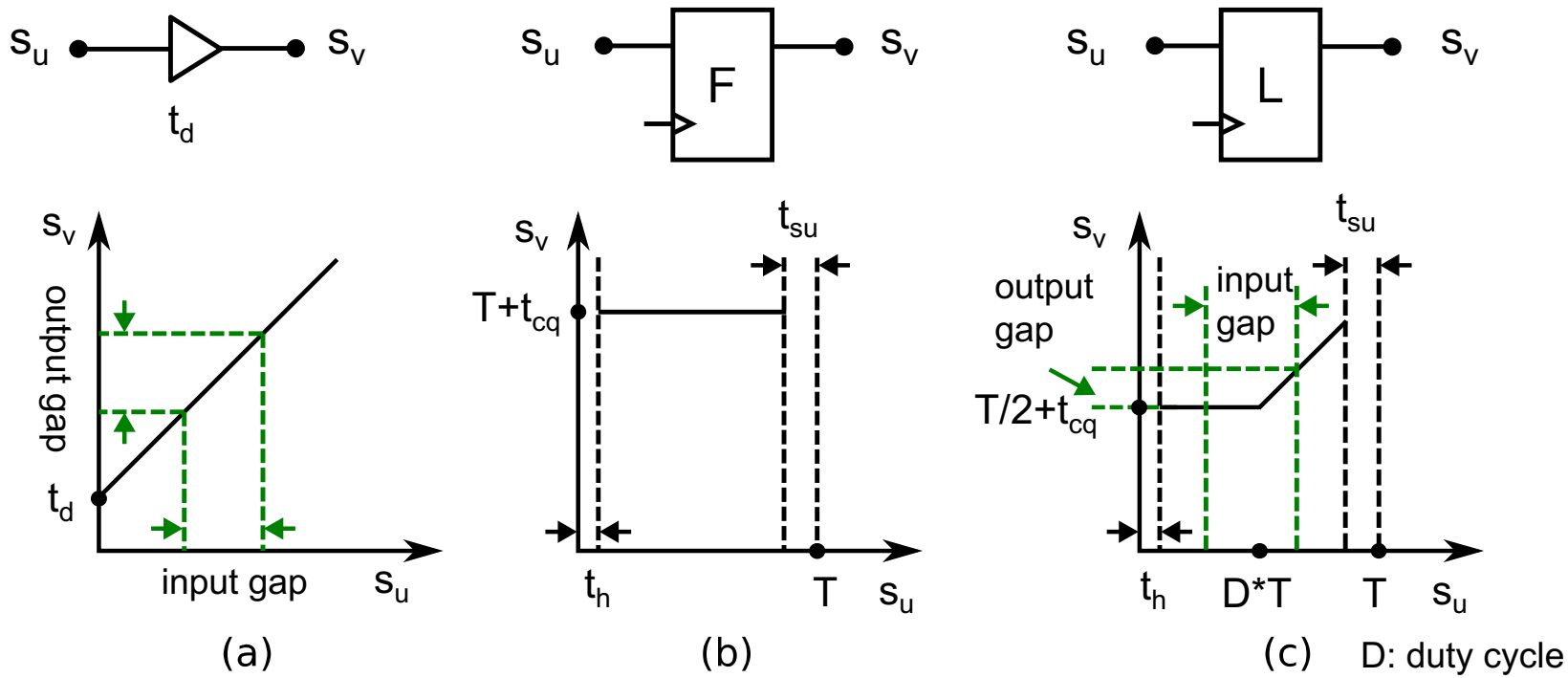
- signals arriving at boundary flip-flops too earlier through fast paths
- signals traveling across combinational loops

# VirtualSync Concept




- **Delay units (logic gates, flip-flops and latches)** are used to slow down signals on fast paths and loops.
- **Reference points** provide relative timing information.

# Generalized Delay Units in VirtualSync



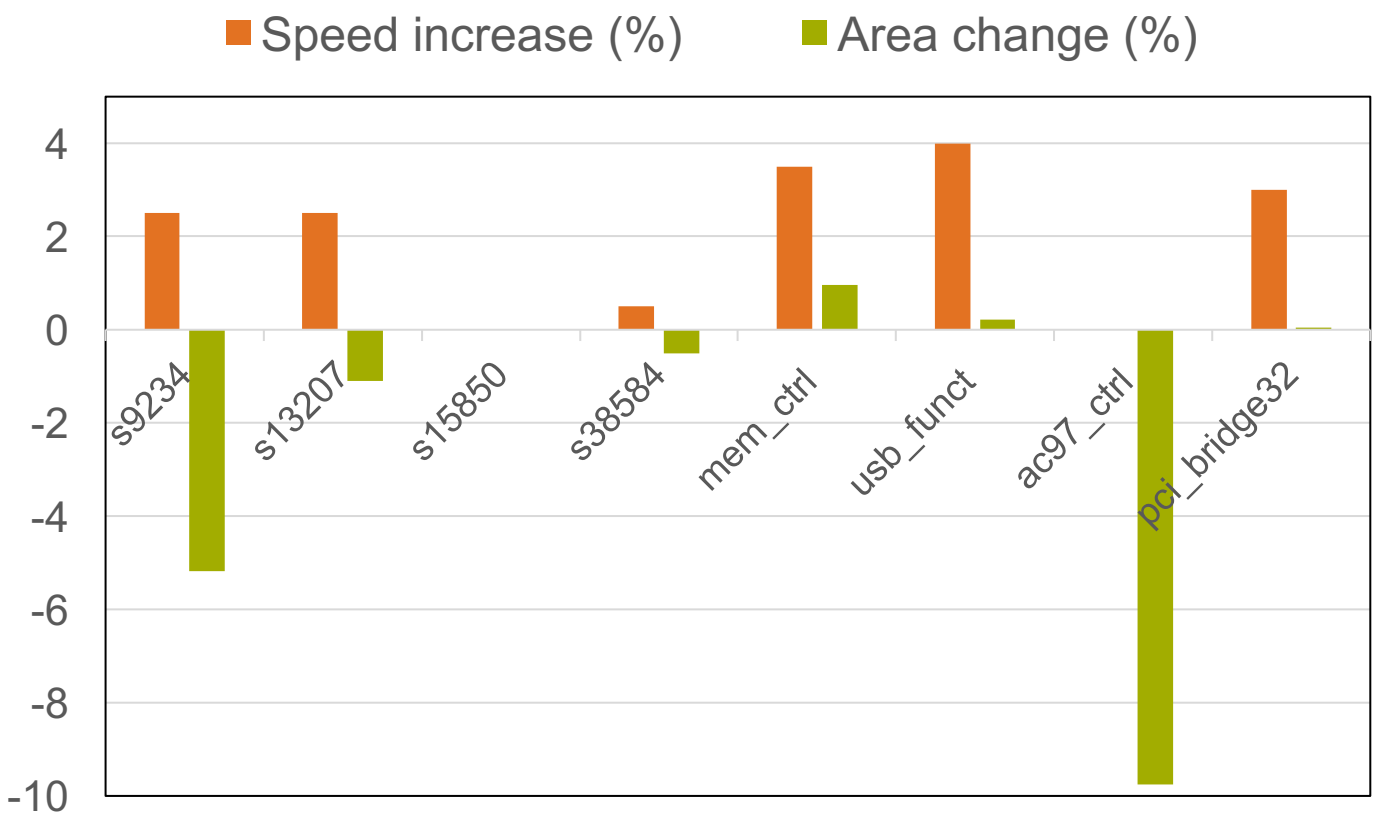

Linear delaying effect of a **combinational gate**

Constant delaying effect of a **flip-flop**

Piecewise delaying effect of a **latch**

Combinational gates, flip-flops and latches are considered as delay units only to slow down fast signals in VirtualSync.

# Results of VirtualSync




Performance increase and area change are compared with ideally balanced design.

# Circuit Counterfeiting by Reverse Engineering

**Counterfeiting threat:** Illegal production of chips by a third party with a netlist recognized through reverse engineering

Authentic chips delayered and imaged

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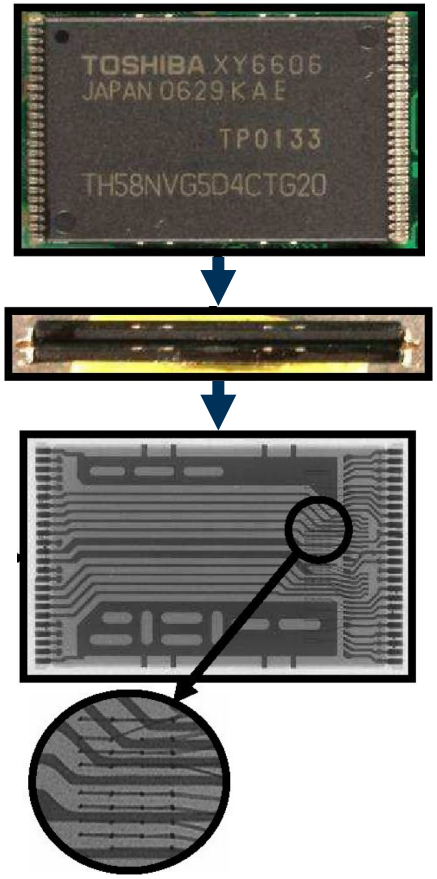
Logic gates, flip-flops and their connections identified

↓

Recognized netlist processed with a standard IC design flow

↓

**Counterfeit chips**

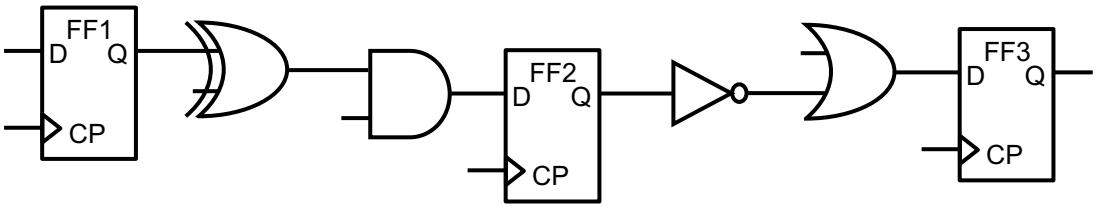



Optical and x-ray images of 64Gb Flash devices



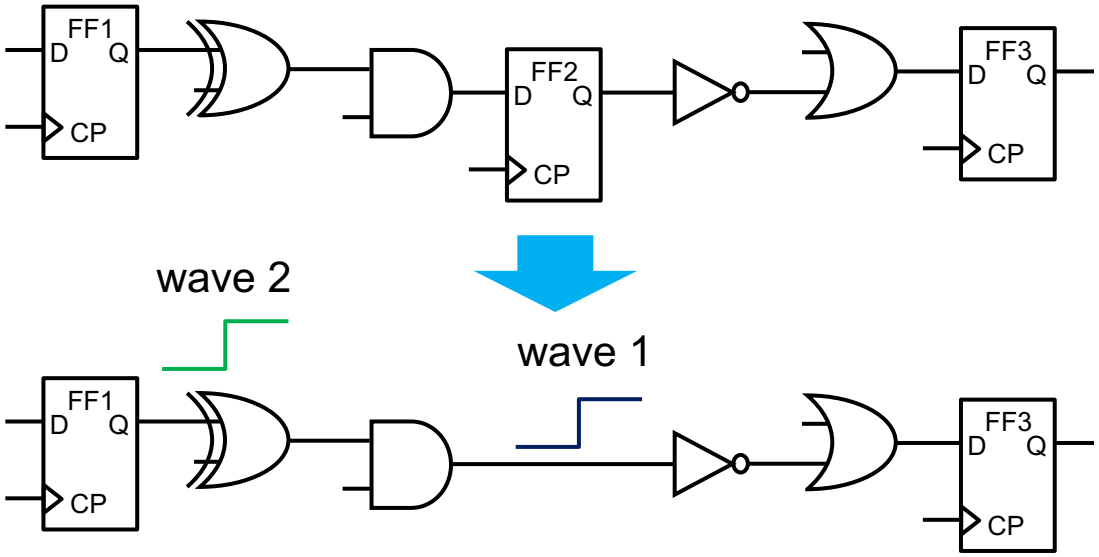
[R. Torrance et al., "Reverse Engineering in the Semiconductor Industry," CICC, Sep, 2007]

# Counterfeiting with Traditional Timing




- Traditional timing model
  - All paths defined with respect to one clock period
  - Setup and hold time constraints satisfied between pairs of flip-flops
- A netlist is sufficient to reproduce a circuit using a standard EDA flow.

# Anti-Counterfeiting with VirtualSync




Timing camouflaged netlist

one logic wave

two logic waves

Recognized circuit loses synchronization

Additional effort to extract timing information

# Summary

- Virtual synchronization with generalized delay units demonstrates a good potential for high-performance designs.
- Timing camouflage opens up a new dimension of circuit netlist security.
- Exploration of design methodologies may improve circuit performance further and benefit interdisciplinary topics such as hardware security.

# Thank you for your attention!