**Invitation to the Oral Examination – Department CE**

For the occasion of her examination for a Doctoral Degree,

**Lei Zhang**

will present her dissertation entitled

**Design of Analog/Mixed-Signal FeFET/SRAM Compute-In-Memory Core with Improved Computational Accuracy**

on **28.04.2026** at **10:00**

Attendance to the presentation is open to the public. The presentation will be in English.

The candidate, all members of the Examination Committee, and authorized examiners of the TUM School of CIT are invited to the presentation and subsequent oral examination.

The presentation and subsequent examination will take place in

**Theresienstr. 90, 80333 München, Room: N1812**

**Examination committee:**

Chair: **Prof. Dr. Hussam Amrouch**

First Examiner: **Prof. Dr. Ralf Brederlow**

Second Examiner: **Prof. Dr. Amelie Hagelauer**

Munich, the **06th** of **April 2026**

**Mailing list:**

Members of the examination committee

Doctoral candidate


## Abstract:

This work proposes criteria and methods for selecting quantization methods, memory technologies, and circuit topologies to meet the target computational accuracy of analog compute-in-memory (CIM) cores. Based on those methods, this work presents two CIM cores with FeFET and SRAM, which reduce the relative INL to approximately 17.7% and 0.30% with energy efficiency of 13.9 - 443 TOPS/Wand 25.4 TOPS/W, respectively. Those are achieved by using 2HVT1 FeFET bitcells and slope-ADC in the FeFET CIM core, and current-steering method in the SRAM core.